NASA-CR-191355

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SBIR- 14.06-6642A
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ADVANCED ON-CHIP DIVIDER FOR MONOLITHIC MICROWAVE VCOs

(NASA-CR-191355) ADVANCED ON-CHIP DIVIDER FOR MONOLITHIC MICROWAVE VCO'S Final Report (Microwave Monolithics) 101 p
N93-13563
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SBIR PHASE II FINAL REPORT
CONTRACT No. NAS7-1000

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MAY 1989

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PROJECT SUMMARY

High frequency division on a monolithic circuit is a critical technology required to significantly enhance the performance of microwave and millimeter-wave phase-locked sources. The approach followed by Microwave Monolithics Incorporated (MMInc.) to meet this need is to apply circuit design practices which are essentially "microwave" in nature to the basically "digital" problem of high speed division. Following investigation of several promising circuit approaches, program phase I culminated in the design and layout of an "8.5 GHz" (Deep Space Channel 14) divide by four circuit based on a dynamic mixing divider circuit approach.

Therefore during program phase II, MMInc. has fabricated and optimized an "8.5 GHz" VCO with an integral divider which provides a phase coherent "2.125 GHz" reference signal for phase locking applications. Complete phase locked operation of the monolithic GaAs devices (VCO, power splitter, and dynamic divider) was demonstrated both individually and as an integrated unit. The fully functional integrated unit in a suitable test fixture has been delivered to NASA for engineering data correlation.

Based on the experience gained from this "8.5 GHz" super component, a monolithic GaAs millimeter-wave dynamic divider for operation with an external VCO was also designed, fabricated, and characterized. This circuit, which was also delivered to NASA, demonstrated coherent division by four at an input frequency of 24.3 GHz.

The high performance monolithic microwave VCO with a coherent low frequency reference output described in this report and others based on this technology will greatly benefit advanced communications systems in both the DoD and commercial sectors. Signal processing and instrumentation systems based on phase-locked loops will also attain enhanced performance at potentially reduced cost.

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1) INTRODUCTION

Advanced deep space probes and communication satellite systems require ultra-stable phase coherent frequency sources for differing but equally critical requirements. Limited prime power (and therefore transmitter power) combined with extreme distances necessitate narrow bandwidth, moderate bit rate communications and highly stable sources for deep space probes. Sophisticated modulation schemes and high data rates in limited bandwidths result in similar source stability requirements for communications satellite systems. Monolithic microwave frequency divider phase locked sources of the type developed by Microwave Monolithics Incorporated (MMInc.) consume less prime power and require less than one-tenth the size and weight of an equivalent MIC source based on multiplier chains, while potentially providing an order of magnitude improvement in phase noise performance. Far better reliability is projected due a lower parts count and far fewer wire bonds and interconnections, thus a significant benefit of this device to NASA is increased longevity of deep space probes and satellites. In addition, in large volumes they can be manufactured at signifcantly lower costs than MIC units.

Key to obtaining a coherent low frequency reference signal suitable for advanced communications systems is development of a monolithic frequency division circuit capable of counting down the output signal of the VCO, which may be as high as millimeter-wave frequencies. The approach selected by MMInc. in SBIR program phase I to meet this need was to apply circuit design practices which are essentially "microwave" in nature to the basically "digital" problem of high speed division. For the SBIR program phase II described herein, the most promising approach to high frequency division, i.e. the mixing divider, was implemented in monolithic form, characterized, and optimized for deep space channel 14. The technique was then extended to millimeter-wave operating bands. At the conclusion of this program, a phase lockable "8.5 GHz" VCO with a coherent reference output at "2.125 GHz" was constructed, characterized, and delivered to NASA to demonstrate the capabilities of this technology. A first iteration monolithic

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millimeter-wave divider chain consisting of a "32 GHz" divider and a second iteration 8.5 GHz divider was also packaged and delivered to NASA to further demonstrate the potential of this technology to impact next generation frequency sources for deep space applications.

Section 2 of this report presents an executive summary describing the objectives, approach, and results of this program. Details of MMInc.'s approach to microwave and millimeter-wave frequency synthesis are presented in section 3, followed by a description of the design, fabrication, and characterization of the 8.5 GHz VCO with integral divider in sections 4, 5 and 6 respectively. An optimized design and its performance characteristics are then presented section 7. The monolithic GaAs millimeter-wave divider and its performance are next described in section 8. The report ends with conclusions and recommendations in section 9.

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2) EXECUTIVE SUMMARY

High frequency division on a monolithic circuit is a critical technology required to significantly enhance the performance of microwave phase-locked sources while simultaneously reducing power consumption and increasing reliability for advanced deep space probes and communication satellite systems. To meet this need, MMInc. has applied circuit design practices which are essentially "microwave" in nature to the basically "digital" problem of high speed division. The design and layout of an "8.5 GHz" (Deep Space Channel 14) divide by four "mixing divider" from program phase I was taken as the starting point for the phase II effort, which had the dual objectives of implementing a channel 14 VCO with integral divider and the demonstration of this technology at millimeter-wave frequencies. MMInc.'s success in meeting these objectives has opened the possibility of a significant breakthrough in microwave coherent source design and fabrication.

During the phase II program, MMInc. has fabricated and optimized an "8.5 GHz" VCO with an integral divider which provides a phase coherent "2.125 GHz" reference signal for phase locking applications. The first iteration design was fully functional, however the operating band was slightly lower than the design value. Utilizing MMInc.'s in-house CAD capabilities and careful characterization of selected MMICs, the cause of these discrepancies was traced and corrective design modifications were identified and implemented. The second iteration designs were fabricated, and the monolithic VCO, monolithic dynamic divider, and a monolithic auxilliary power splitter all functioned as desired. Following integration of the three monolithic components, phase locked operation of the resulting super component was realized. The fully functional integrated "8.5 GHz" VCO super component with integral phase coherent sub-harmonic reference output capable of operation at deep space channel 14 has been delivered to NASA.

Based on the experience gained from this "8.5 GHz" super component, a monolithic GaAs dynamic divider for operation with an external 31.86225 GHz VCO (to provide an "8 GHz" coherent reference

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signal) was also designed, fabricated, and characterized. After further division with the "8 GHz divide by four, the resulting reference output would be readily compatible with conventional high speed digital dividers and phase locking technology. Following fabrication and characterization it was determine that, as occurred for the initial 8.5 GHz MMICs, the operating band was lower than the design goal. Design modifications necessary to correct these performance variations have been identified, however program constraints did not permit their implementation. None the less, the performance of this first iteration millimeter-wave divider, at a slightly reduced frequency, clearly indicates the potential of MMInc.'s approach to microwave and millimeter-wave freqeuncy synthesis. This divider was fixtured as the high frequency front end of a divider chain, which was delivered to NASA as an integrated unit.

Monolithic microwave frequency dividers of the type developed by MMInc. thus open the possibility of low power, highly stable, high reliability, phase locked sources for a wide range of deep space probes and/or communications satellites.

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3) MONOLITHIC MICROWAVE FREQUENCY SYNTHESIS

To obtain frequency synthesizers operating in the high microwave and millimeter-wave bands, low frequency synthesized sources must be coherently "up converted" by one of several means. Three major approaches, or a combination of them, are applied for this purpose: 1) Frequency multiplication, 2) Mixing with a fixed high frequency source, or 3) Phase locking of a counted down fundamental frequency VCO. The first requires high prime power and extensive filtering, and demonstrates rapidly deteriorating phase noise characteristics (6 dB degradation per octave of frequency multiplication). The second requires a stable high frequency source near the desired operating frequency, which is almost as difficult to attain as the final objective. Extensive filtering is often necessary as well. The latter is clearly the preferred approach, provided that a suitable frequency divider exists.

Flip-flops are traditionally used for "digital" frequency division, with each stage halving its input frequency. At clock speeds well below the gate delays of the technology in use, other division ratios are implemented by appropriate combinational logic and feedback schemes. These approaches, which are well documented in the literature, require small substrate areas and provide acceptable power dissipation for most VCO applications. However, current digital GaAs technology has a practical frequency limit of between 2 and 4 GHz. Although the exact upper limit deemed attainable over the next five or ten years is subject to debate, it is not expected to exceed Ku-Band frequencies without a breakthrough in device technology. Even allowing the possibility of such a breakthrough, operation at high microwave or millimeter-wave frequencies is not considered serious at the present time. These devices are, however, quite flexible at frequencies below 2 GHz. The dynamic dividers developed under this program will therefore act as pre-scalers for the microwave and/or millimeter-wave VCOs, with their output feeding more traditional "digital" dividers. These, in turn, will feed the phase comparator of a phase locked loop.

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Prior to a detailed description of MMInc.'s frequency division circuits, it should be noted that these circuit approaches complement rather than conflict with advances in device technology. As improved conventional MESFETs, as well as advanced devices such as HEMTs and Heterojunction Bipolar Transistors (HBJT), become more mature from laboratory R&D efforts towards viable technologies, the same circuit techniques are expected to further increase the maximum division frequency, possibly reaching far into the millimeter-wave frequency range. At the lower frequencies, use of these techniques will relax required device geometries, thereby enhancing yield and reducing costs. Direct division by a large number in one step also potentially reduces prime power requirements at the lower frequencies.

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4) DESIGN OF 8.5 GHz DIVIDER WITH INTEGRAL VCO

4.1) 8.5 GHz Monolithic Dynamic Divide by Four

4.1.1) Circuit Design

In program phase I, MMInc. identified a mixing divider as the best frequency division approach for this application due to its high performance, low power consumption, and the prospect of extension to millimeter-wave frequencies.

A mixing divider is a non-linear circuit which regeneratively supports the desired sub-harmonic oscillation in response to a driving input signal. The initial sub-harmonic signal exists as part of the broadband noise present in all electronic circuits, and with sufficient positive feedback this signal rapidly grows high above the noise floor, reaching steady state at saturation of the non-linear element(s) in the circuit. The most common form of this type of circuit is the halver shown in Figure 4.1.1-1, where the first sub-harmonic mixes with the input signal to regenerate itself provided the phase shift (time delay) around the loop results in positive feedback and the amplifier gain overcomes losses associated with the mixer. A variation of this circuit allows the generation of other division ratios as shown in Figure 4.1.1-2. In this case, for an input signal f_o, signals f_o/N and $f_o(N-1)/N$ are both supported. The phase shift and gain must now be correct at both the desired output frequency and the idler frequency, while as many other mixing products as possible (as well as the input frequency) should inherently cancel. For linear phase shift (constant time delay) feedback networks, the latter is achieved when the division ratio is even, therefore even N should usually be a design goal. Note that the halver is a special case of this circuit with N=2. In this case the idler and output frequencies are one and the same.

The output sampling circuit must select the desired low frequency and suppress the others while not loading down the feedback loop. Note that as the division ratio is increased, the idler frequency approaches

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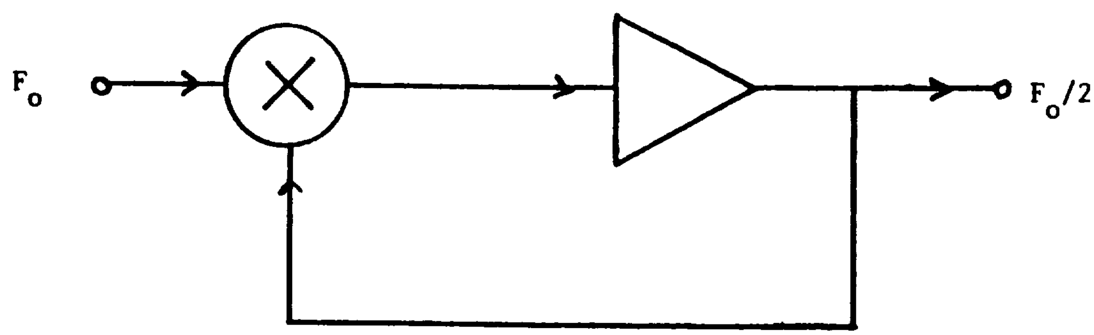

Figure 4.1.1-1) Schematic of a Frequency Halving Circuit.

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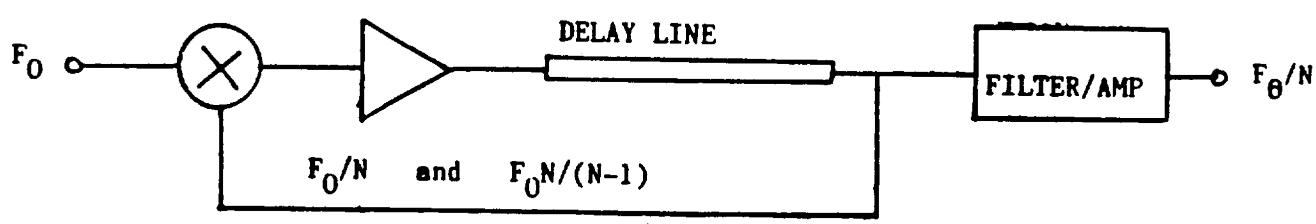

Figure 4.1.1-2) A Variation of the Halver Which Allows the Generation of Other Division Ratios.

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the input frequency and other undesirable mixing products approach the output frequency, putting a practical limit on the frequency scaling possible with a single dividing stage. Gain elements are then required near the input frequency, necessitating high performance active devices. Bandwidth is also reduced as the division ratio is increased. The amount of division is therefore circuit an input frequency dependent, however values of four or six appear attractive. Although the mixer, loop amplifier, delay network, and output sampling circuit are conceptually distinct, there is a large degree of interaction in the in the actual circuit design. For example, the amplifiers and output sampling introduce delay, and the active mixer provides some of the loop gain.

A schematic diagram of the 8.5 GHz mixing divider developed under this program is shown in Figure 4.1.1-3. Predicted gain and phase shift of the buffer amplifier are shown in Figures 4.1.1-4 and 4.1.1-5 respectively. Note that the phase shift is very close to linear phase, allowing phase adjustment of over the multi-octave loop bandwidth with a simple delay line. An alternate loop amplifier design, with gain and phase response shown in Figures 4.1.1-6 and 4.1.1-7 respectively, was also considered for this application. As shown, this amplifier provided a notch to suppress the undesired divide by two frequency, however the phase response was extremely difficult to compensate and sensitivity to circuit parameter variations was high. Therefore this circuit was not pursued.

The layout generated to implement this monolithic GaAs divider circuit is shown in Figure 4.1.1-8. Key features of the design are the active loads on the mixer and amplifiers for high gain with small chip area, and a source follower (common drain) output sampling circuit which has high input impedance for minimal loading of the regenerative loop. A low pass output filter helps suppress undesired harmonics of the divide by four output signal which must be present in the regenerative loop. Included on-chip are all necessary bias and bypass circuitry to make it insensitive to external supply impedances. The divider chip is 2 millimeters long and 1.5 millimeters high for a total chip area of

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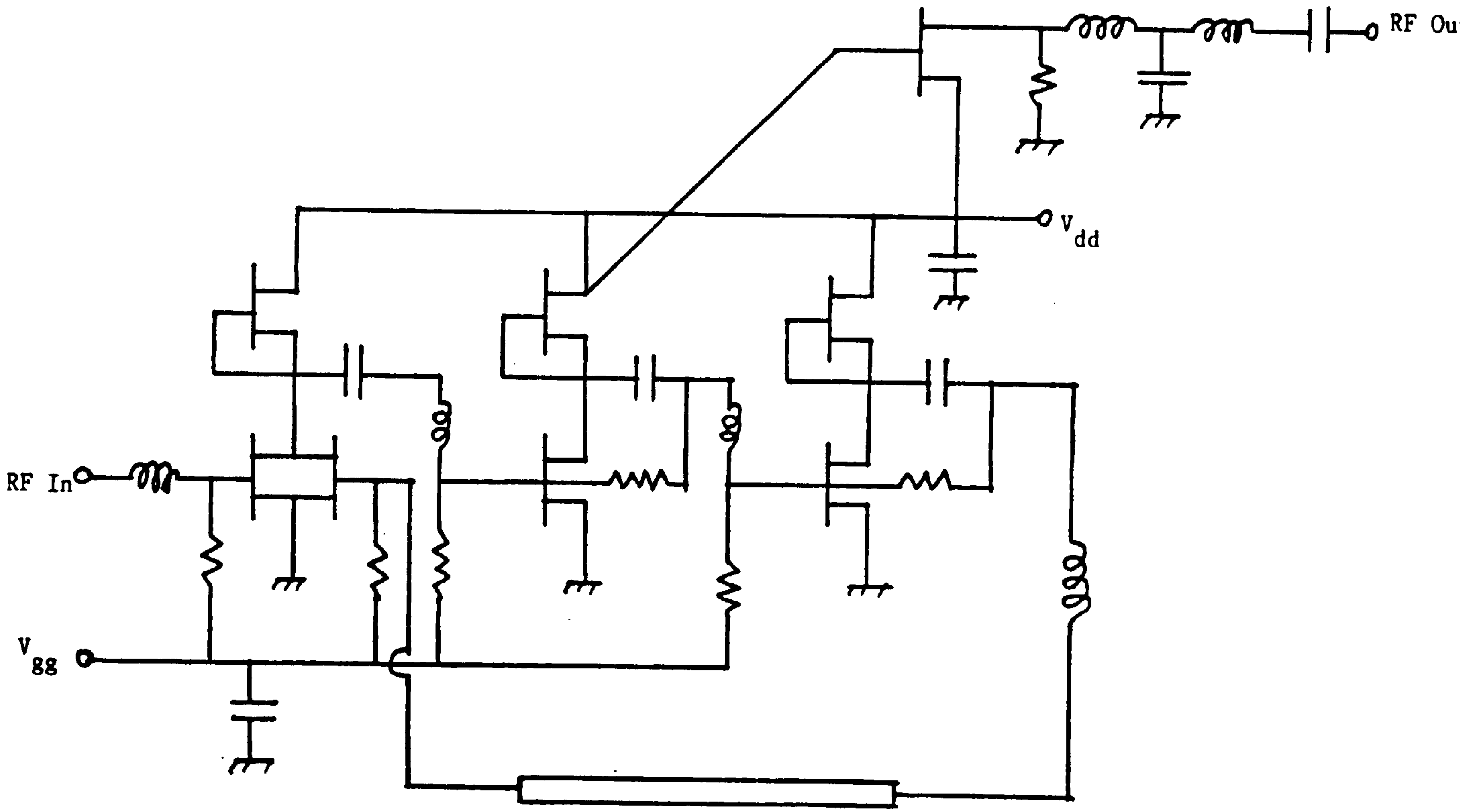

Figure 4.1.1-3) Schematic Diagram of the 8.5 GHz Mixing Divider.

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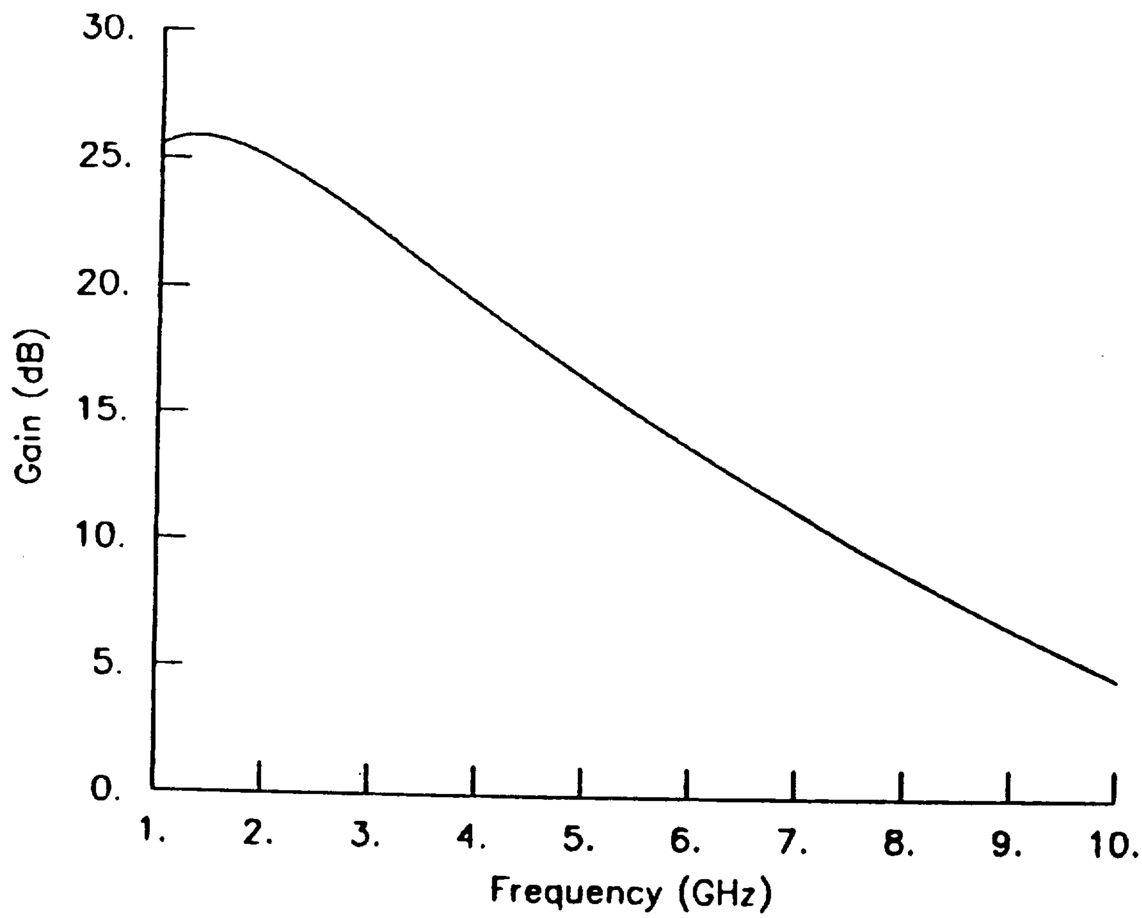

Figure 4.1.1-4) Predicted Small Signal Gain of the Loop Amplifier.

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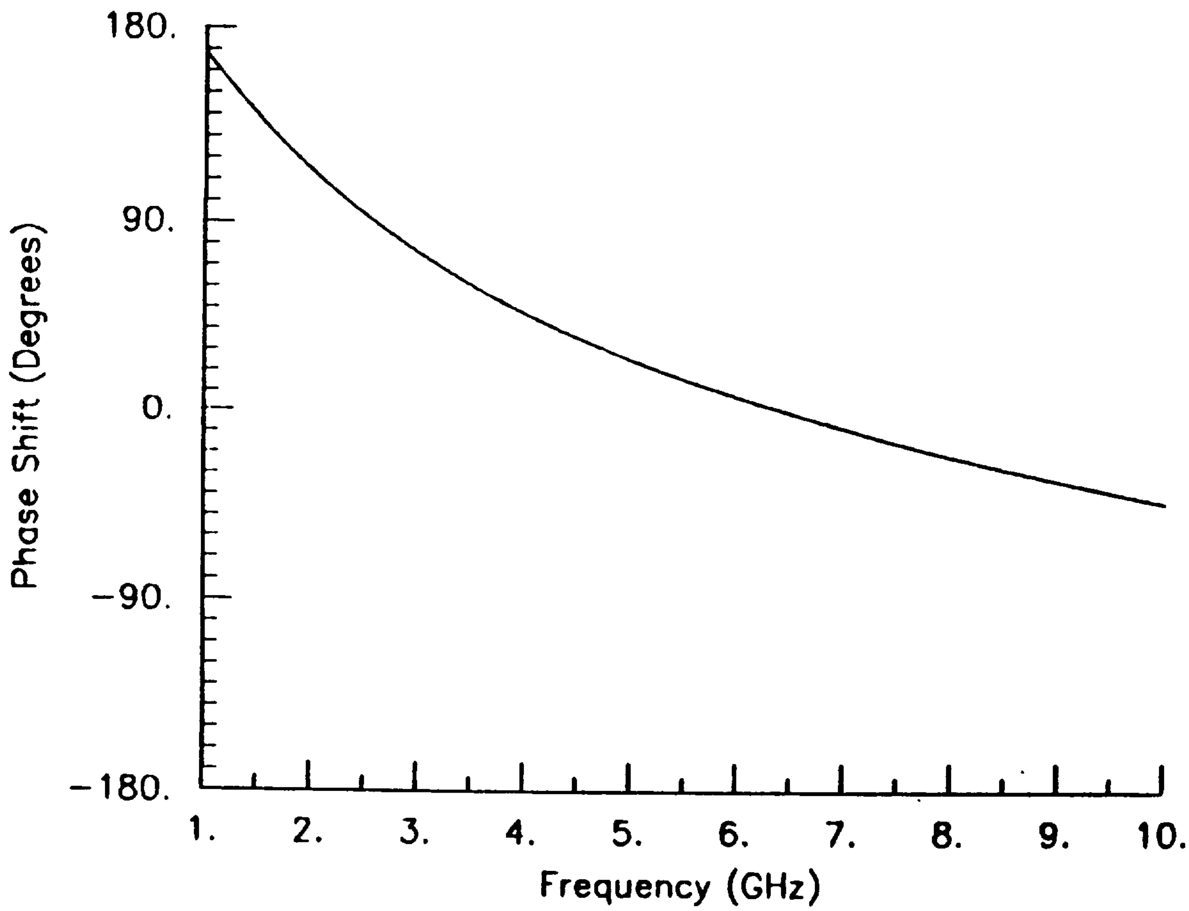

Figure 4.1.1-5) Predicted Small Signal Phase Shift of the Loop Amplifier.

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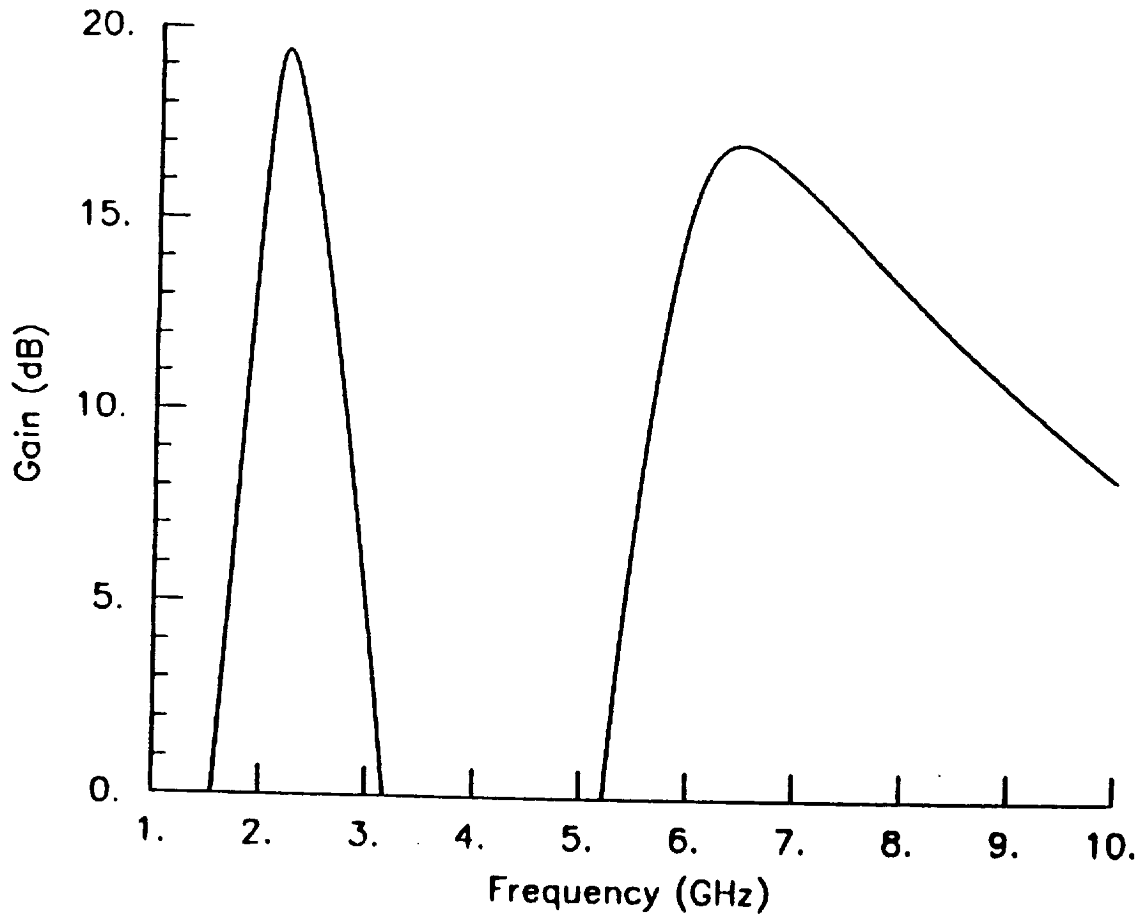

Figure 4.1.1-6) Predicted Small Signal Gain of the Alternate Design Loop Amplifier.

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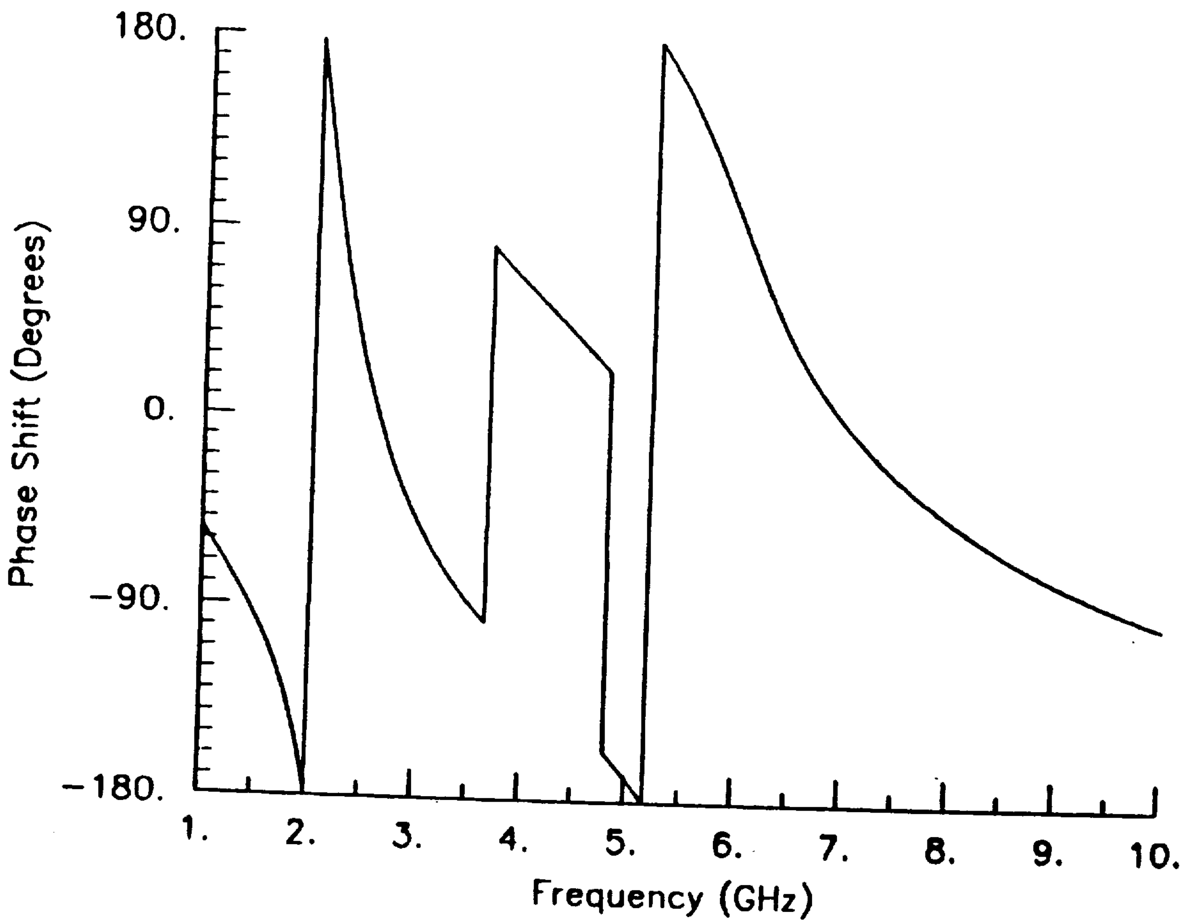

Figure 4.1.1-7) Predicted Small Signal Phase Shift of the Alternate Design Loop Amplifier.

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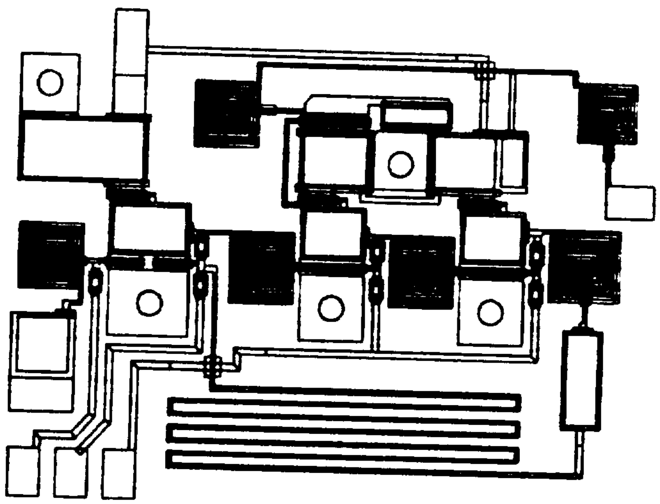

Figure 4.1.1-8) Layout of the 2 millimeter by 1.5 millimeter 8.5 GHz Mixing Divider. This 3 square millimeter MMIC chip includes eight FETs, six spiral inductors, nine capacitors, eight resistors, and 5 through substrate via holes in addition to the 3 DC bias bonding pads and two RF bonding pads.

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3 square millimeters. It includes eight FETs (with 3/4 micron gate length and varying gate width), six spiral inductors, nine capacitors, eight resistors, and five through substrate via holes in addition to the three DC bias bonding pads and two RF bonding pads. A long delay line near the bottom of the chip provides the necessary additional time delay (phase shift) for re-generation of the 2.125 GHz output signal and the 6.375 GHz idle frequency necessary for proper operation.

4.1.2) Predicted Divider Performance

Large signal circuit simulation of the divider were performed using the proprietary computer program "MMIC-SPICE", a modified and enhanced version of SPICE2. The built-in device models in MMIC-SPICE accurately account for both the current-voltage relationship and the voltage dependence of the capacitances, which is essential for simulation of these highly non-linear circuits.

Predicted performance of the complete divider circuit is summarized in Figures 4.1.2-1a through 4.1.2-1e. In this set of figures, the RF output signal frequency is plotted against input frequency for several different input power levels. Each point in this set of figures represents one MMIC-SPICE simulation followed by a discrete fourier transformation to the frequency domain. The MMIC-SPICE time domain simulation extends to six nanoseconds to reach steady state, and the fourier transform then generates an output spectrum to determine if proper locking has occurred. The total simulation summarized in Figure 4.1.2-1 required over 30 VAX/780 equivalent CPU hours to complete. From these figures, the locking range at each input power level is easily identified. Predicted RF output power is plotted as a function of input power at an input frequency of 8.5 GHz in Figure 4.1.2-2. Note that there is actually a conversion gain produced by this circuit.

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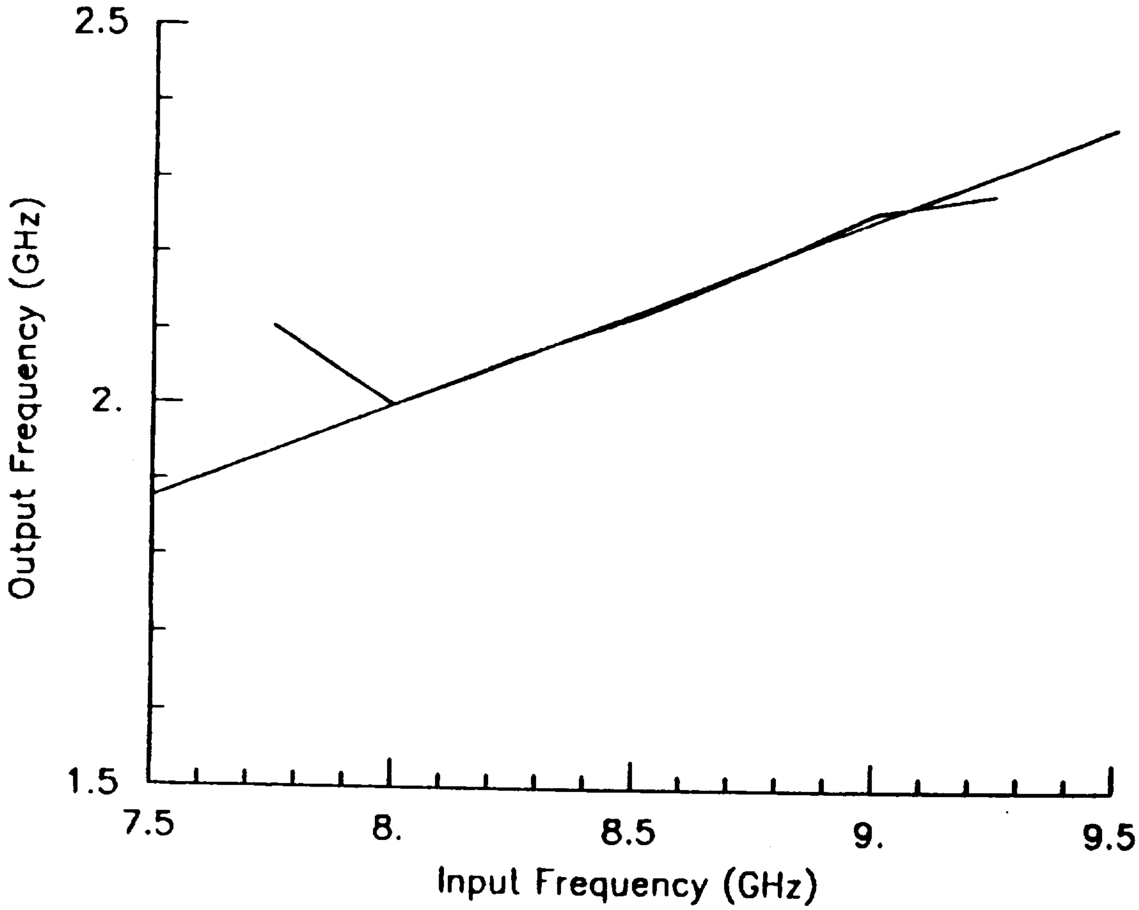

Figure 4.1.2-1a) Predicted Output Frequency Plotted as a Function of Input Frequency for the 8.5 GHz Mixing Divider at an Input Power of 10 dBm.

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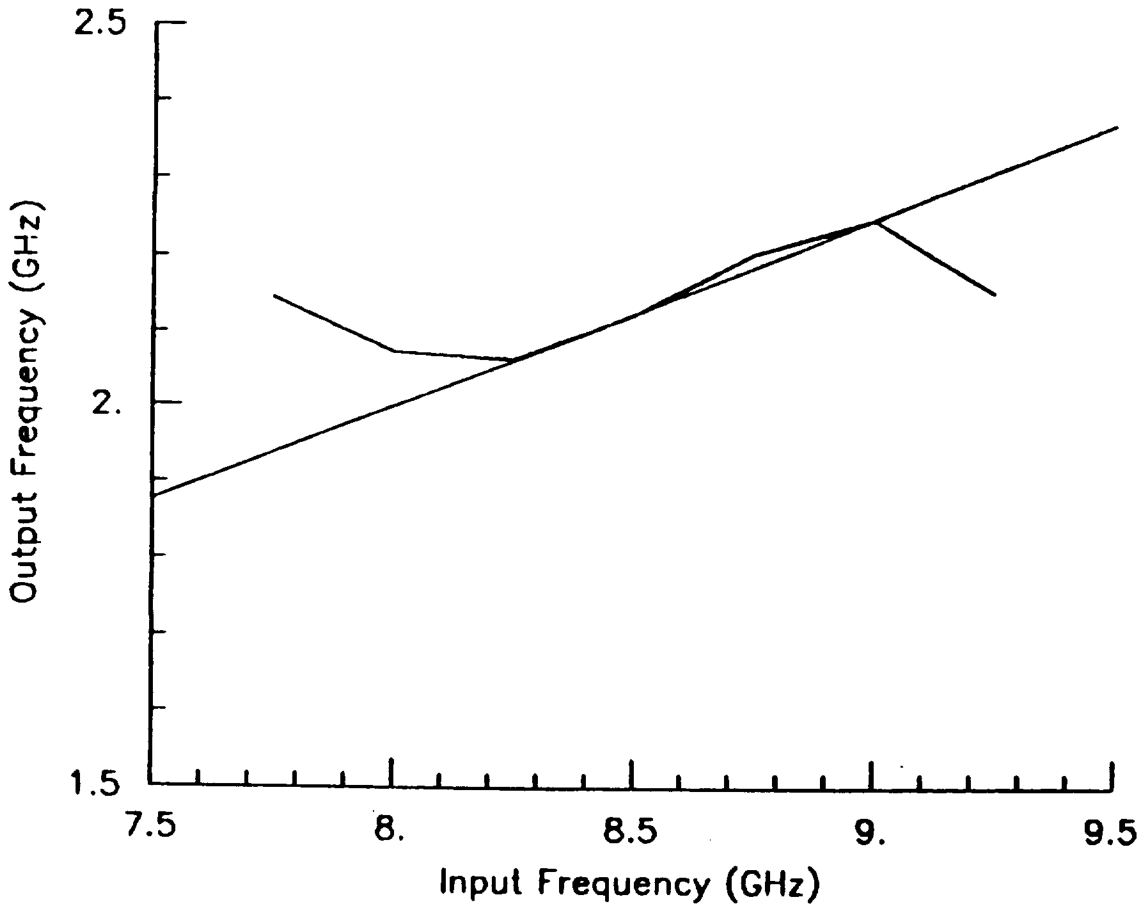

Figure 4.1.2-1b) Predicted Output Frequency Plotted as a Function of Input Frequency for the 8.5 GHz Mixing Divider at an Input Power of 7.5 dBm.

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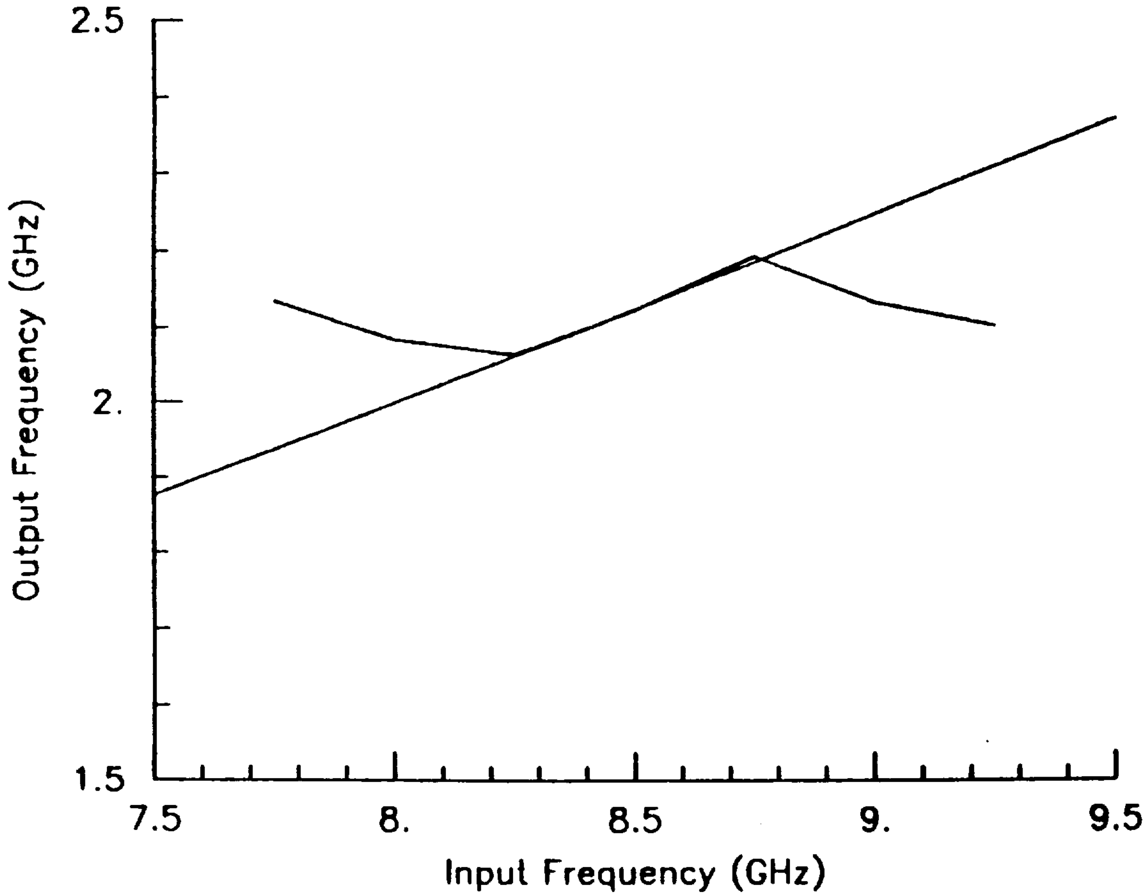

Figure 4.1.2-1c) Predicted Output Frequency Plotted as a Function of Input Frequency for the 8.5 GHz Mixing Divider at an Input Power of 5dBm.

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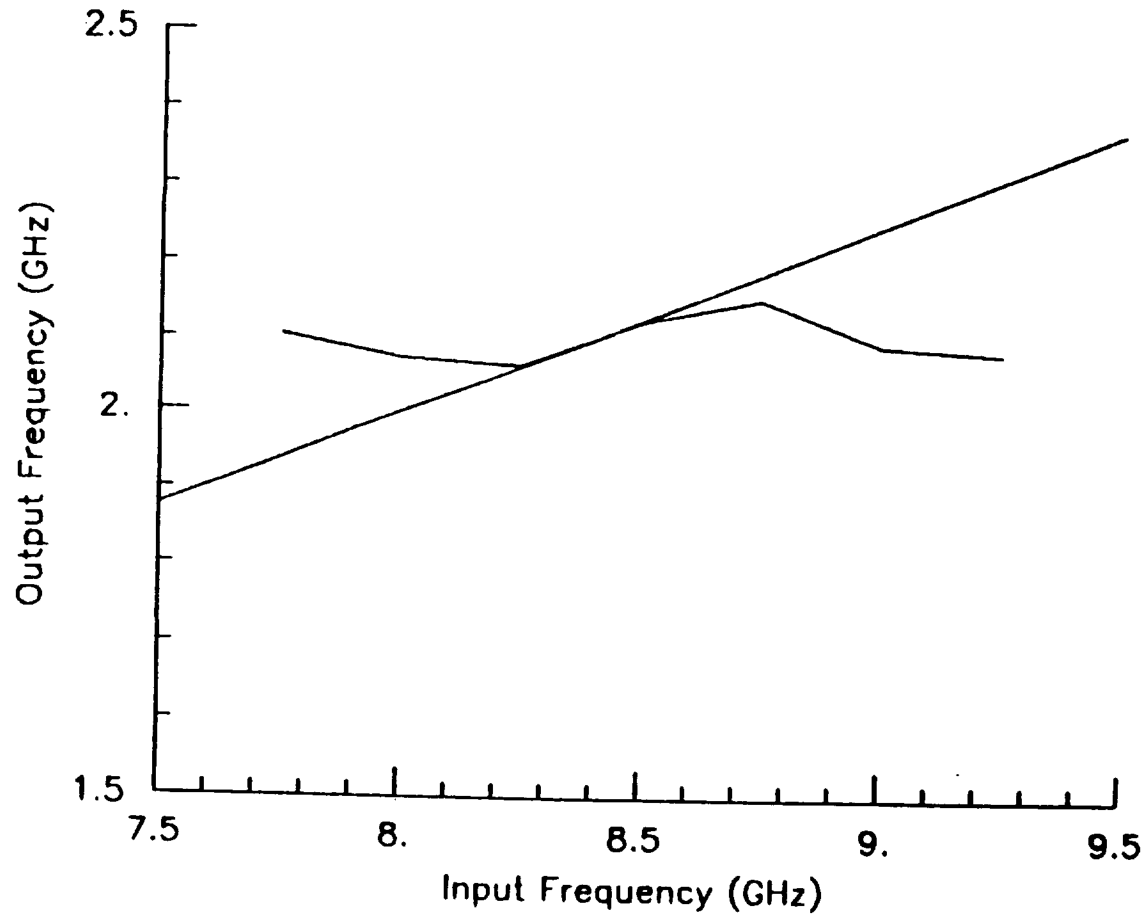

Figure 4.1.2-1d) Predicted Output Frequency Plotted as a Function of Input Frequency for the 8.5 GHz Mixing Divider at an Input Power of 2.5 dBm.

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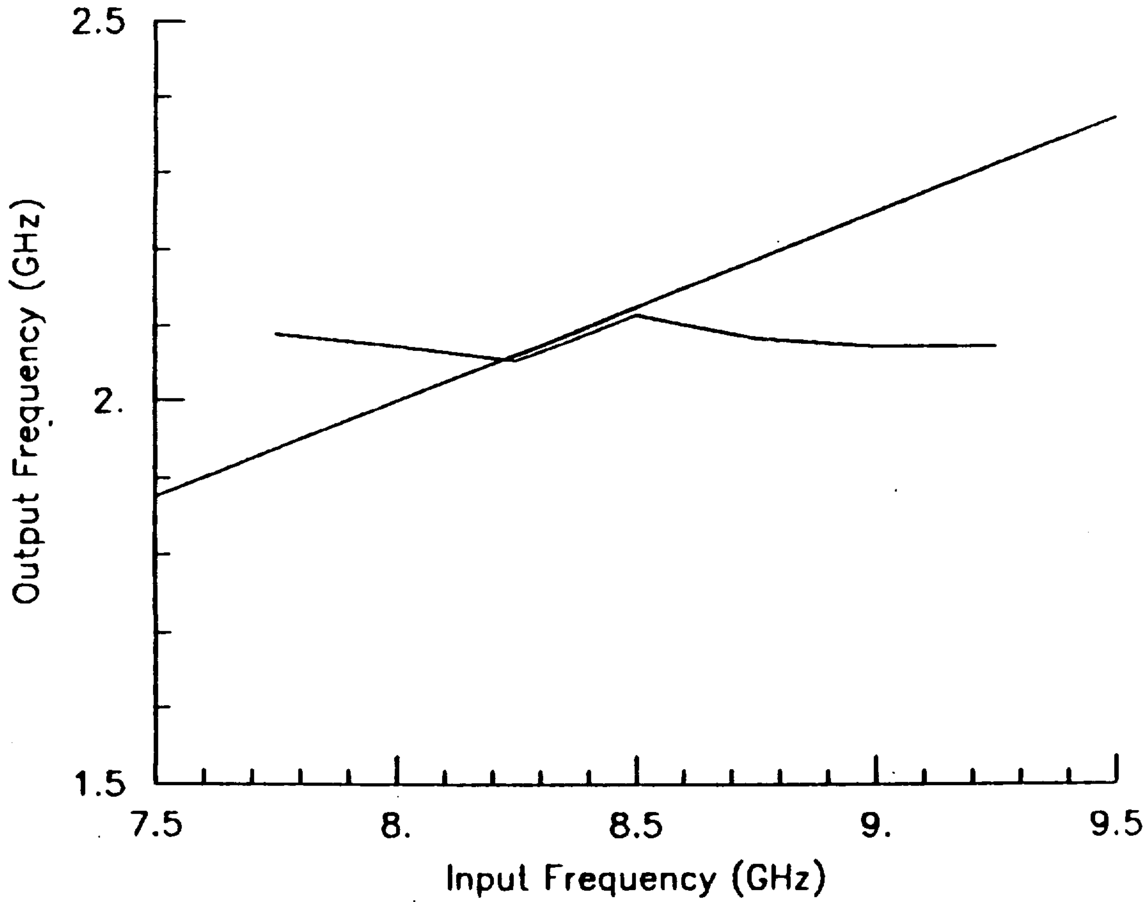

Figure 4.1.2-1e) Predicted Output Frequency Plotted as a Function of Input Frequency for the 8.5 GHz Mixing Divider at an Input Power of 0 dBm.

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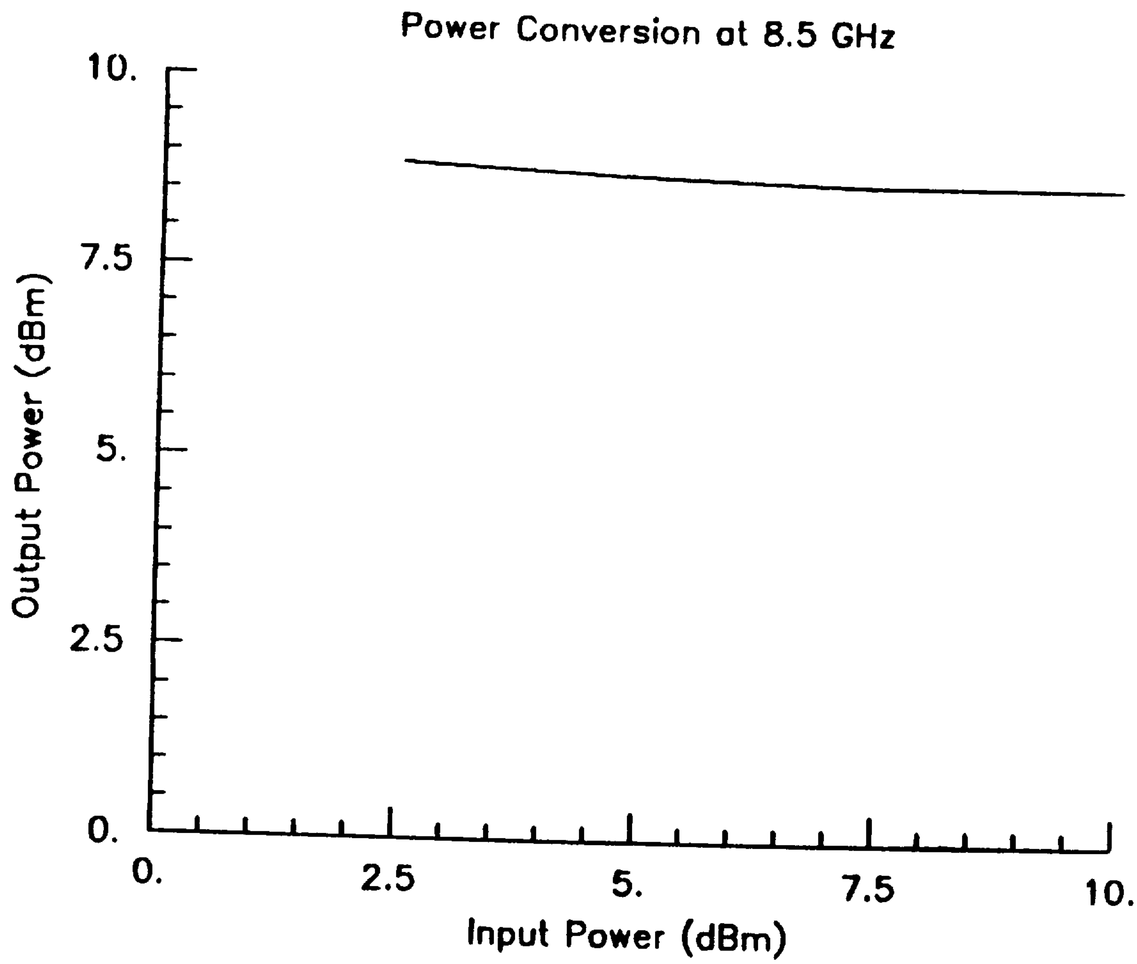

Figure 4.1.2-2) Predicted Output Power as a Function of Input Power at 8.5 GHz for the Mixing Divider.

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Figure 4.1.2-3 shows a typical predicted output waveform under locked conditions. This figure corresponds to an input power of 7.5 dBm at 8.5 GHz, which is one of the points plotted in Figure 4.1.2-1. Predicted DC power consumption for this case is just 549 milliwatts. Figure 4.1.2-4 shows the computed output spectrum for this waveform. Note that the the width of the spectral line and the low level sidebands are artifacts of the numerical transformation and the finite time sample, and that they are not indicative of actual circuit noise performance. Accurate simulation of the noise performance is not feasible with this approach, therefore noise evaluation is best determined experimentally. Note also that the outputs at 4.25, 6.375, and 8.5 GHz are considerably suppressed by the on-chip output filtering circuitry and loop cancellation effects as desired.

In Figure 4.1.2-5, predicted output power is plotted as a function of input power at an input frequency of 8.5 GHz. Note that output power is relatively flat due to the saturated operating mode of this divider circuit.

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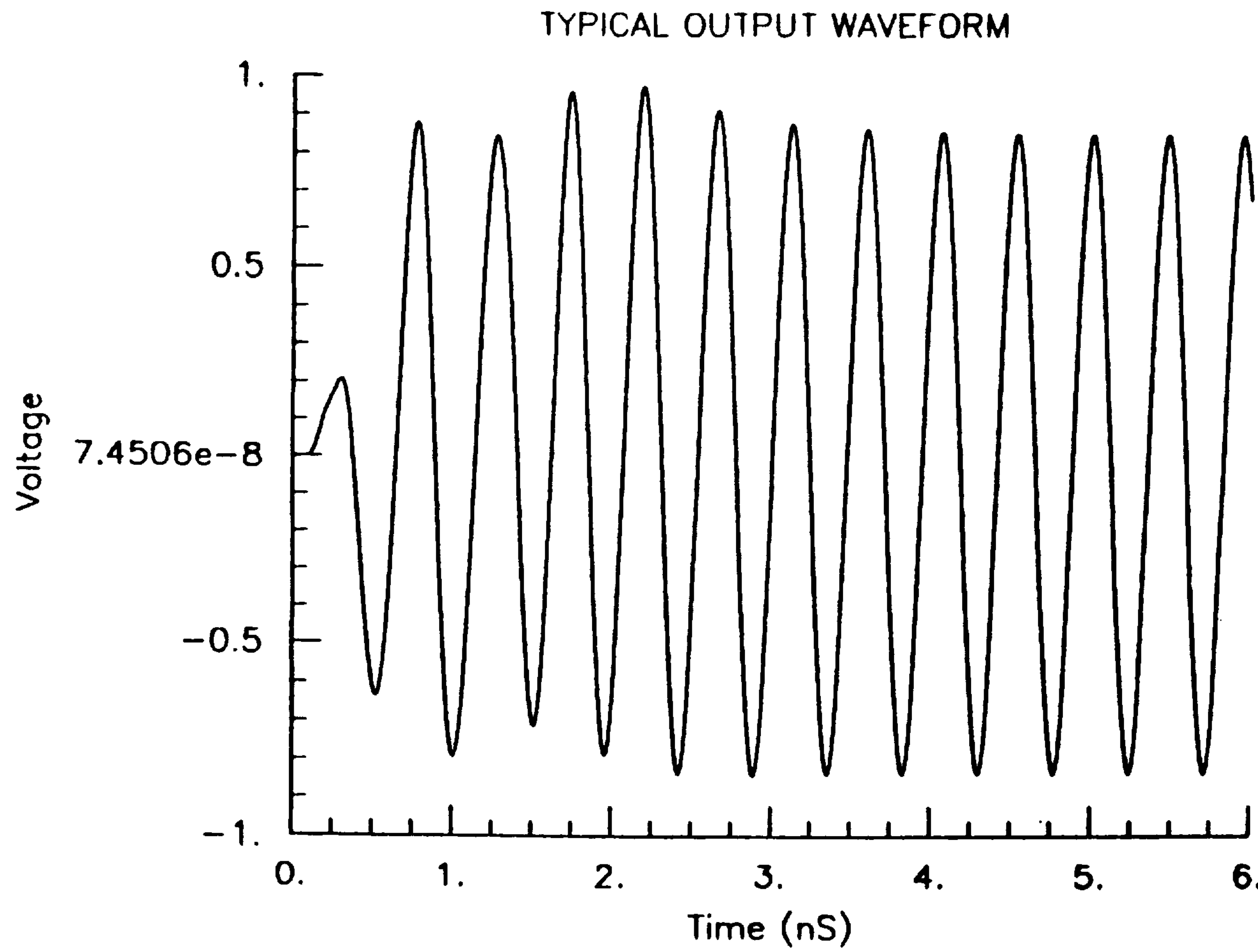

Figure 4.1.2-3) Predicted Output Waveform of the Mixing Divider with an Input Power of 7.5 dBm at 8.5 GHz.

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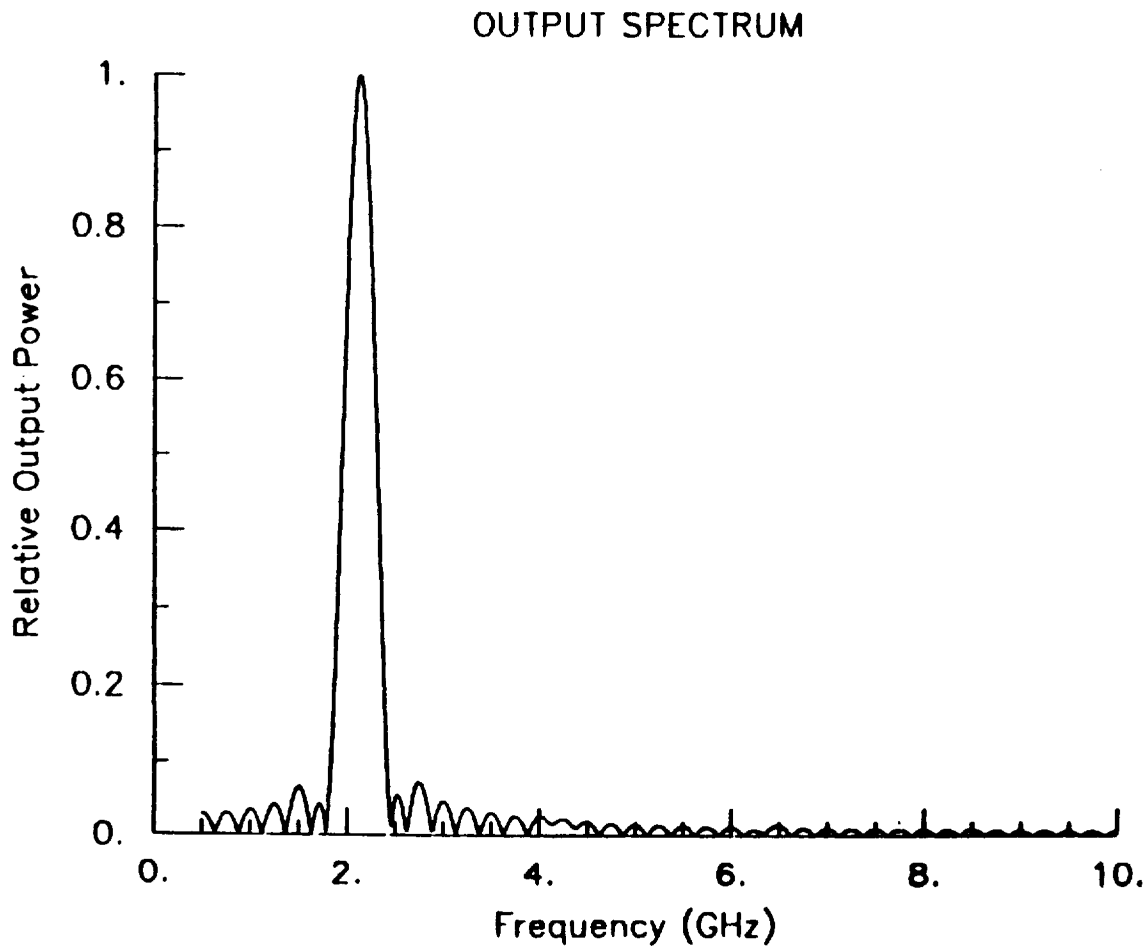

Figure 4.1.2-4) Predicted Output Spectrum of the Mixing Divider with an Input Power of 7.5 dBm at 8.5 GHz.

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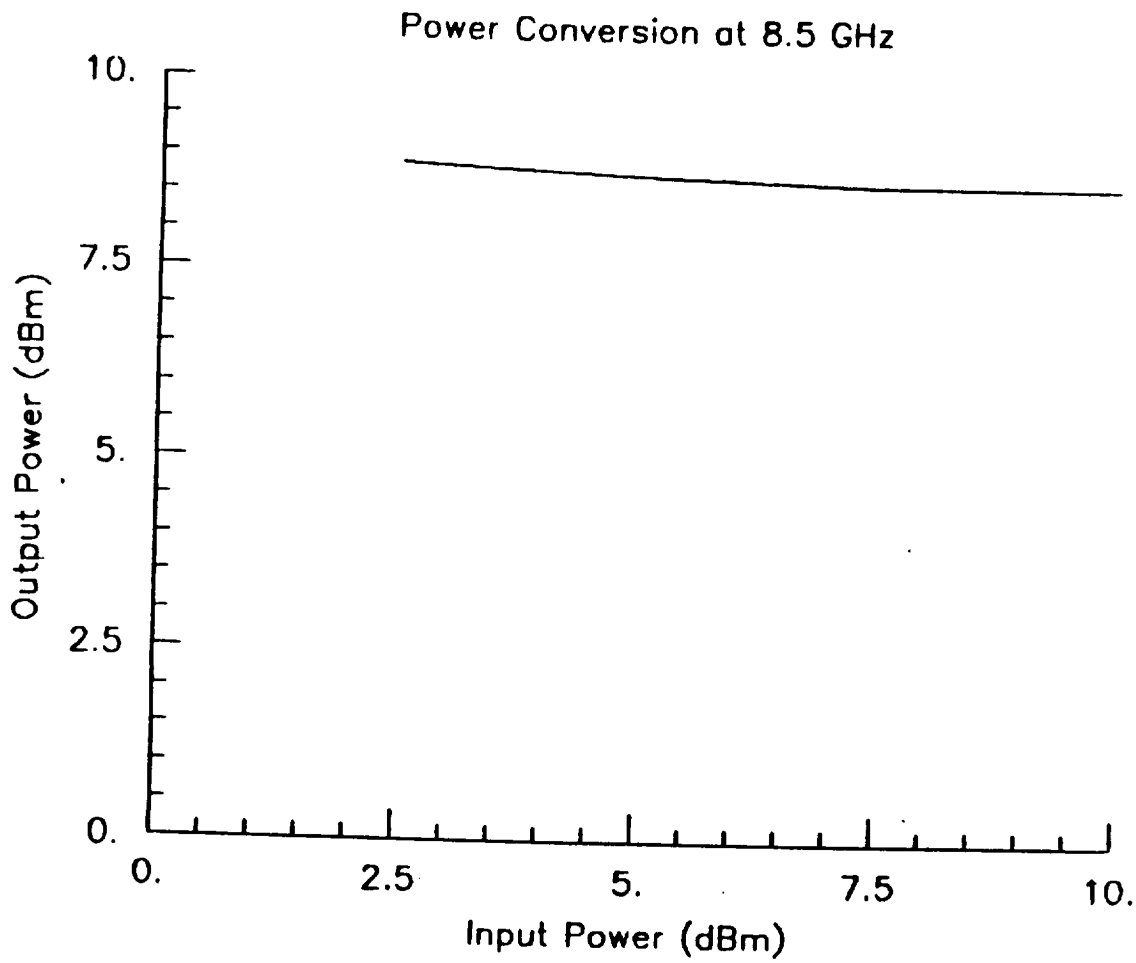

Figure 4.1.2-5) Predicted Power Conversion Characteristics of the Mixing Divider at an Input Frequency of 8.5 GHz.

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4.2) 8.5 GHz Monolithic VCO

4.2.1) Circuit Design

Although there are many possible X-band oscillator configurations, there is one that is particularly attractive for practical realization of microwave oscillators - the common drain oscillator. In this configuration an appropriate source impedance, in combination with the augmented parasitic capacitances of the FET, is utilized to provide a negative resistance at both the gate and drain terminals. Therefore the source inductance, which is usually a harmful parasitic element, becomes part of the matching network. A tunable frequency determining resonator is then placed at the gate electrode and power is taken from the drain. A buffer amplifier provides additional output power, load pull isolation, and a well defined load to the oscillating FET device.

A schematic diagram of the monolithic 8.5 GHz GaAs VCO developed under this program is shown in Figure 4.2.1-1. An on-chip low Q spiral inductor in combination with the gate capacitance of the oscillator FET forms the 8.5 GHz resonator, which is tunable by the gate bias voltage. An interstage matching network, a common source buffer amplifier, and its output matching network complete the circuit design.

A pen plot of this GaAs VCO is shown in Figure 4.2.1-2. Bias and bypass circuitry are on-chip, and the processing sequence is fully compatible with the divider circuitry described above. The 1.1 by 0.9 millimeter chip contains two FETs (each with a gate length of 3/4 microns and gate width of 400 microns), three spiral inductors, six capacitors, three resistors, and two through substrate via holes in addition to the output RF port, single DC supply, and the tuning voltage input bonding pad. The single supply voltage is possible since both the oscillator FET and the buffer amplifier are self biased with source resistors. The source of the oscillator FET is RF isolated with an inductor, therefore no bypass capacitor is needed for its source resistor.

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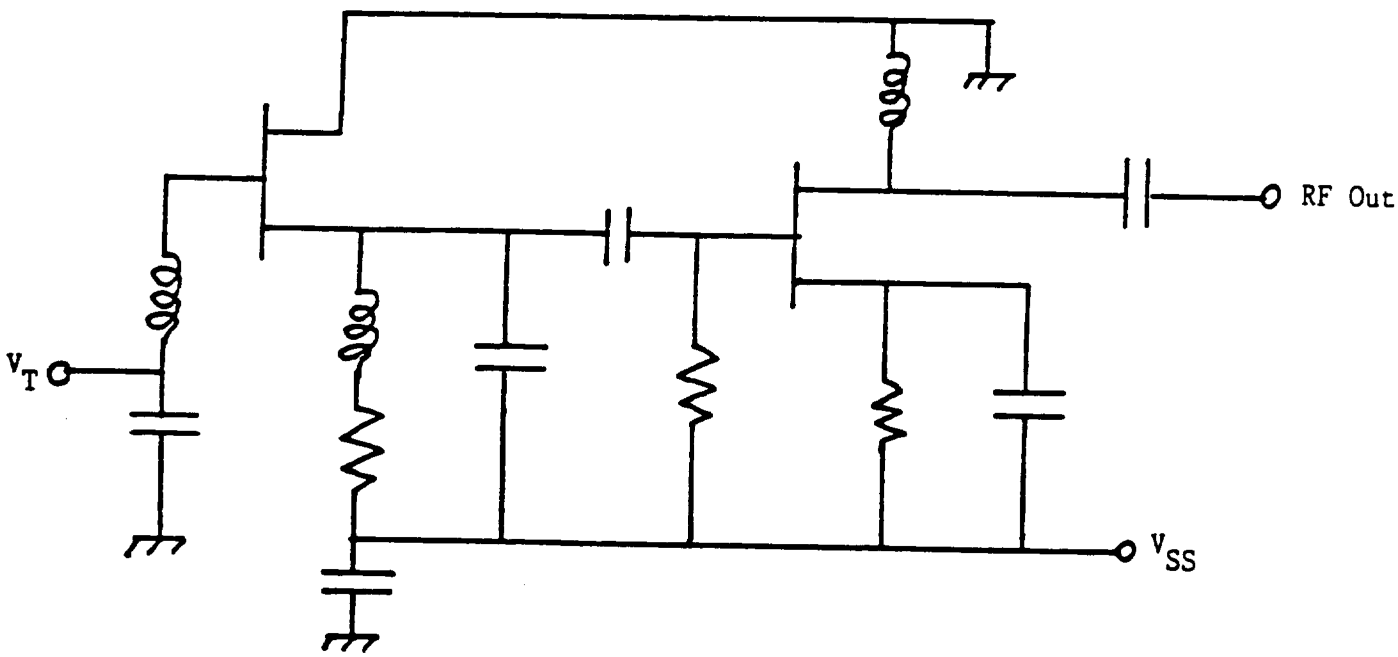

Figure 4.2.1-1) Schematic Diagram of the Monolithic GaAs 8.5 GHz Voltage Controlled Oscillator.

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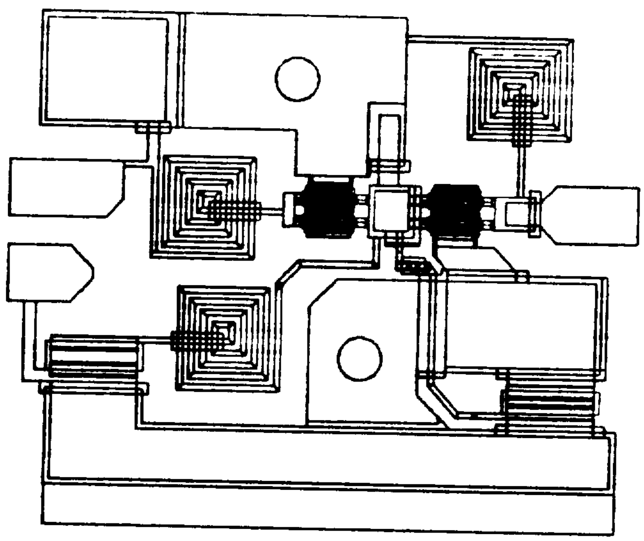

Figure 4.2.1-2) Layout of the 1.1 by 0.9 millimeter monolithic GaAs 8.5 GHz voltage controlled oscillator. This MMIC contains two FETs, three spiral inductors, six capacitors, three resistors, and two through substrate via holes in addition to the output RF port, single DC supply, and the tuning voltage input bonding pad.

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4.2.2) Predicted VCO Performances

Predicted output frequency vs. gate bias voltage for the monolithic 8.5 GHz VCO is shown in Figure 4.2.2-1. Although the predicted tuning range of the VCO as analyzed by MMIC-SPICE covers several gigahertz of bandwidth, the tuning range of the actual device will be much less for a number of reasons. The major reason is the reduced maximum to minimum capacitance ratio of the reverse biased gate to source diode due to model inaccuracies of the device and circuit parasitic capacitances. Although as much care as possible is taken to model these capacitances, the goal of minimizing chip size invariably leads to higher capacitances and reduced tuning range. The difficulties in accurately modeling spiral inductors in close proximity to other circuit elements also contributes to loss in tuning range.

For this reason, an MMIC component is always designed to perform over a wider bandwidth than necessary. The VCO for this application is no exception, since the actual required operating band is well below one gigahertz. In fact, even the predicted bandwidth of the frequency divider, which will be driven by the VCO, is well below the predicted tuning range of the VCO.

As shown in Figure 4.2.2-2, predicted output power over frequency is not significantly degraded by this tuning approach due to the high gain buffer amplifier on-chip. Actual measured power is, however, anticipated to be lower than predicted due to the the overly optimistic loss model currently employed in MMIC-SPICE.

A typical predicted output spectrum is shown in Figure 4.2.2-3. Note that as for the divider, the apparent near carrier "noise" is due to numerical artifacts of the fourier transform rather than a prediction of actual noise performance. RF measurement is necessary to determine noise performance, which is expected to moderate due to the low Q resonator. Phase locking with the aid of the divider will be utilized to stabilize the frequency and suppress near carrier noise.

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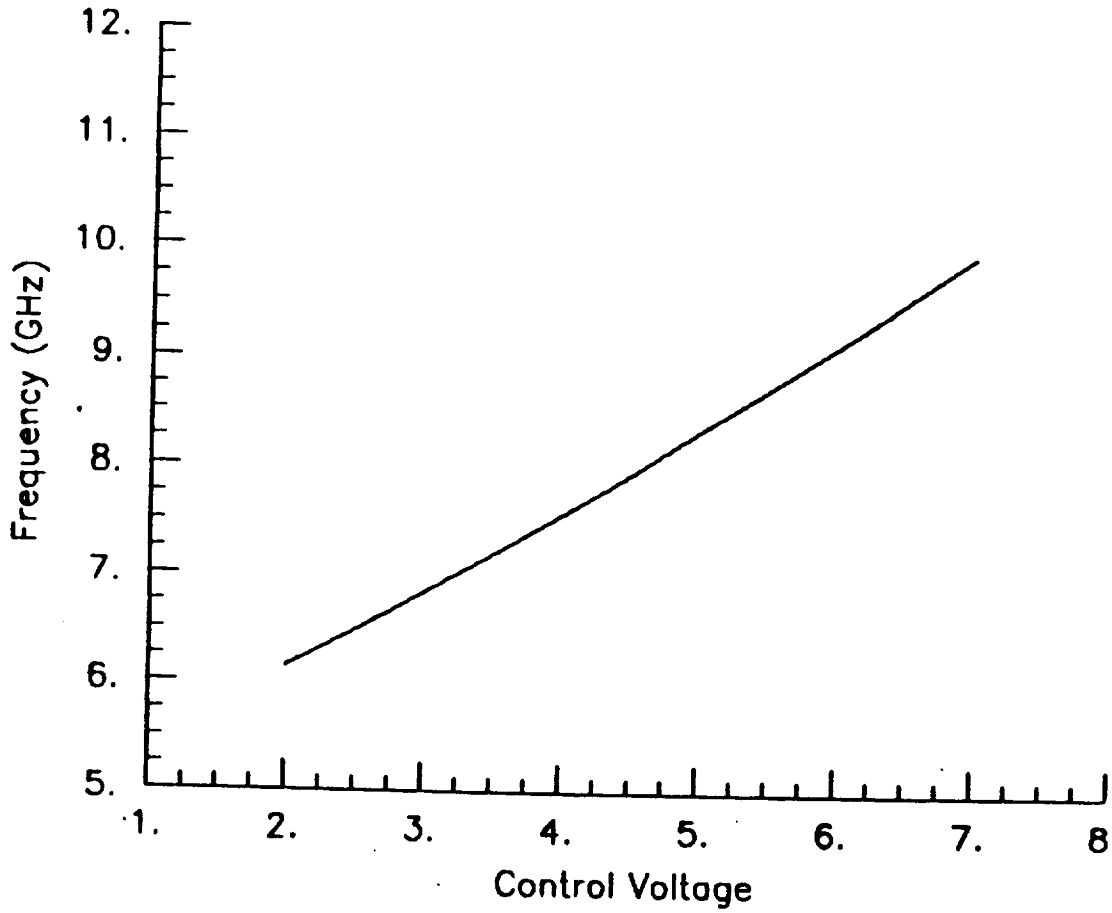

Figure 4.2.2-1) Predicted Output Frequency verses Tuning voltage for the Voltage Controlled Oscillator.

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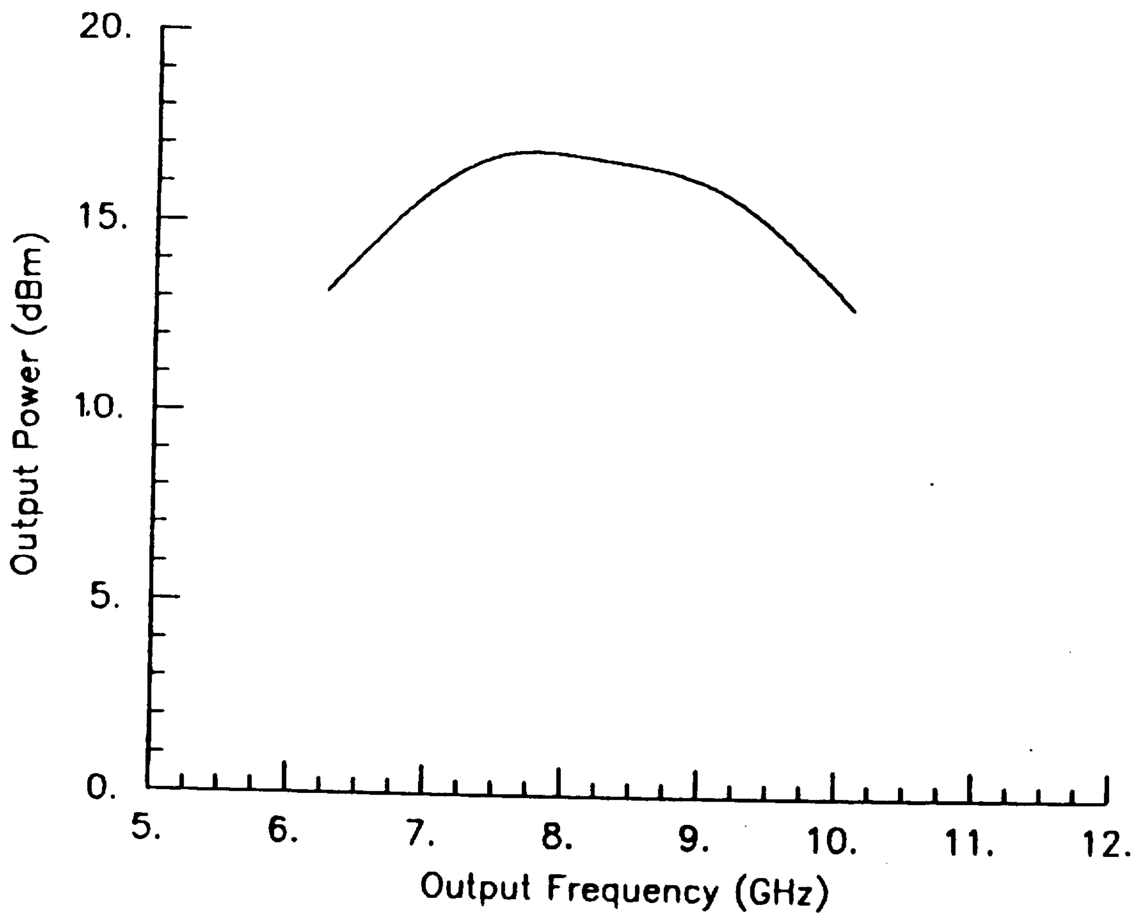

Figure 4.2.2-2) Predicted Output Power verses Output Frequency for the Monolithic Voltage Controlled Oscillator.

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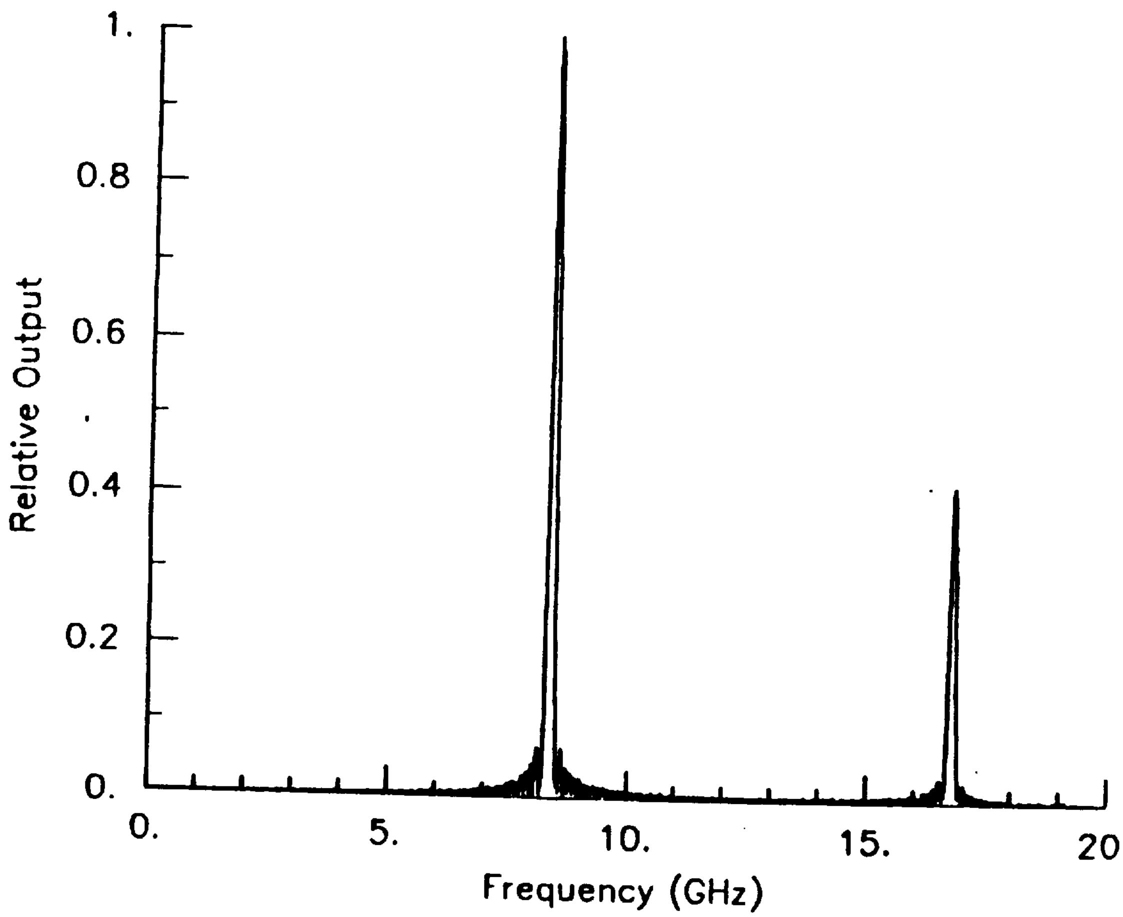

Figure 4.2.2-3) Typical Predicted Output Spectrum for the Voltage Controlled Oscillator.

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4.3) 8.5 GHz Power Splitter

An 8.5 GHz 3 dB power splitter was also designed under this program. This device is intended to send half of the VCO output power to the divide by four circuit, and the other half to the outside world via a 50 ohm microstrip line. It is essentially a standard Wilkinson splitter, except that a slow wave structure is used for each of the the 70 ohm quarter wavelength lines to conserve GaAs real estate. This low pass structure consists of a shunt capacitor, a series inductor (spiral), and a final shunt capacitor. As a result, MMIC chip size is held to just 0.65 by 0.59 millimeters. A schematic of this device is shown in Figure 4.3-1, and the corresponding pen plot layout is shown in Figure 4.3-2.

Predicted performance of the passive monolithic power splitter is summarized in Figures 4.3-3 and 4.3-4. As shown in Figure 4.3-3, this auxiliary circuit provides a 3 dB power split around the 8.5 GHz operating frequency of the voltage controlled oscillator. One output is routed to the divider for signal sampling while the second is the output port of the combined VCO/divider. Predicted input and output match are summarized in Figure 4.3-4.

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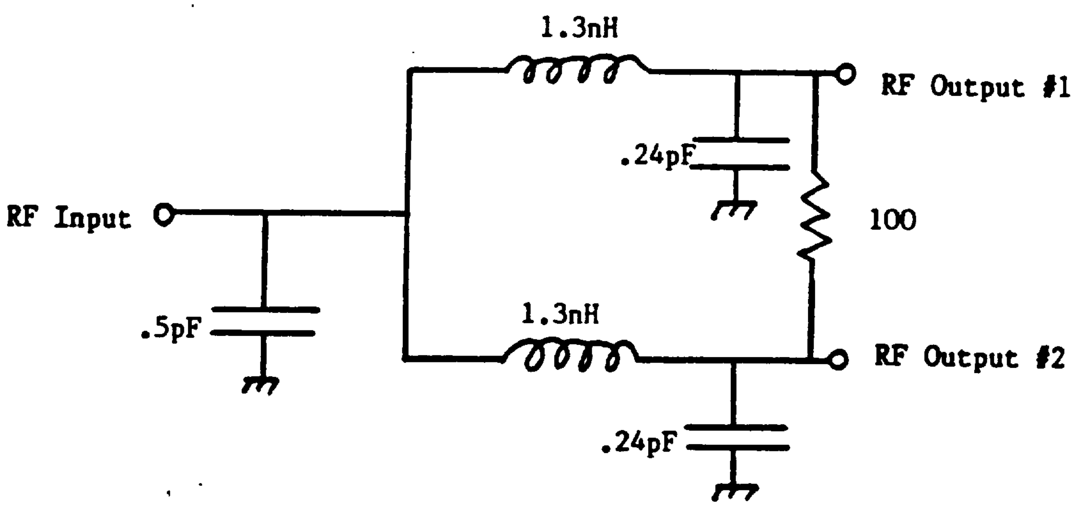

Figure 4.3-1)   Schematic of the 8.5 GHz 3 dB Power Splitter.

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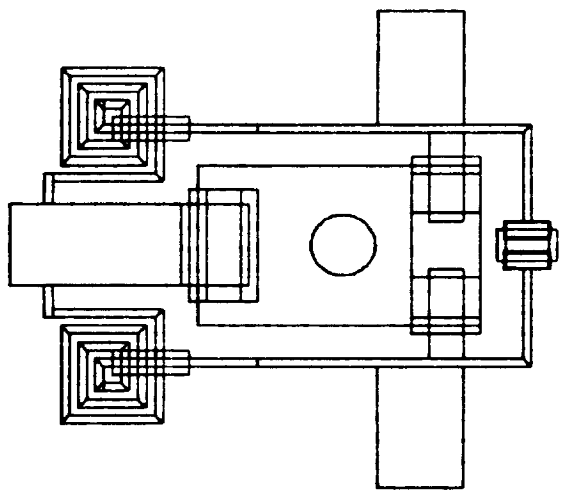

Figure 4.3-2) Layout of the 0.65 by 0.59 millimeter 8.5 GHz 3 dB Power Splitter.

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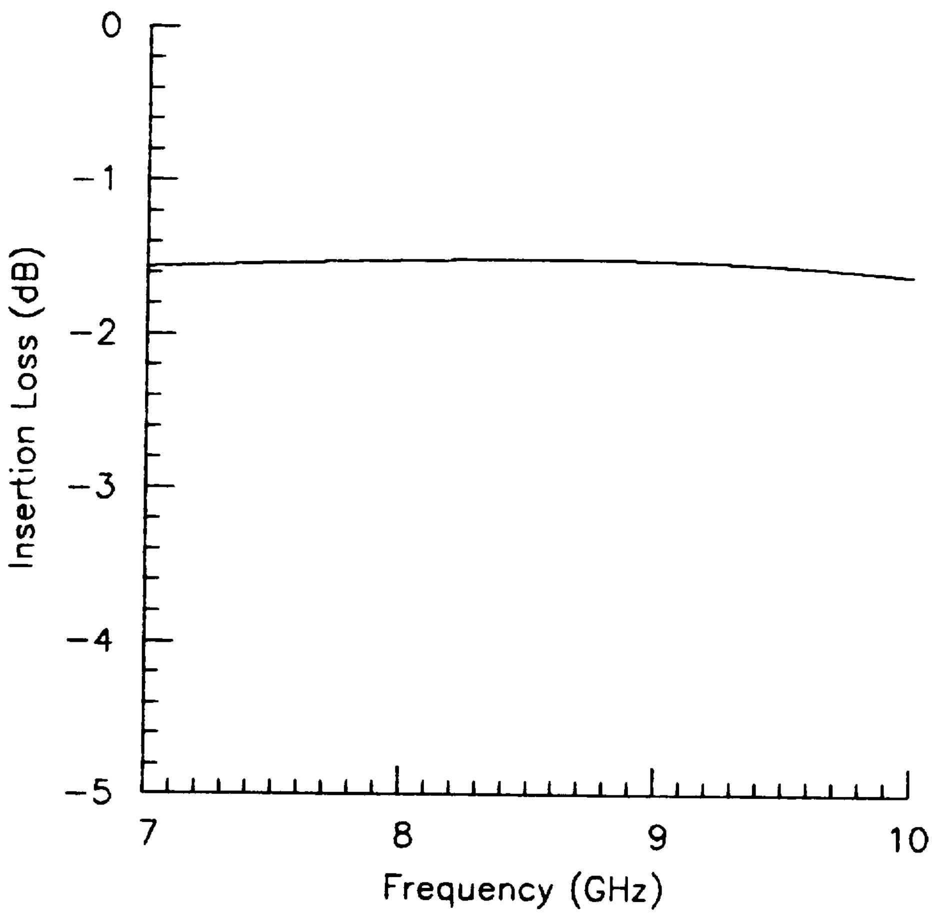

Figure 4.3-3) Predicted Frequency Response of the 8.5 GHz 3 dB Power Splitter.

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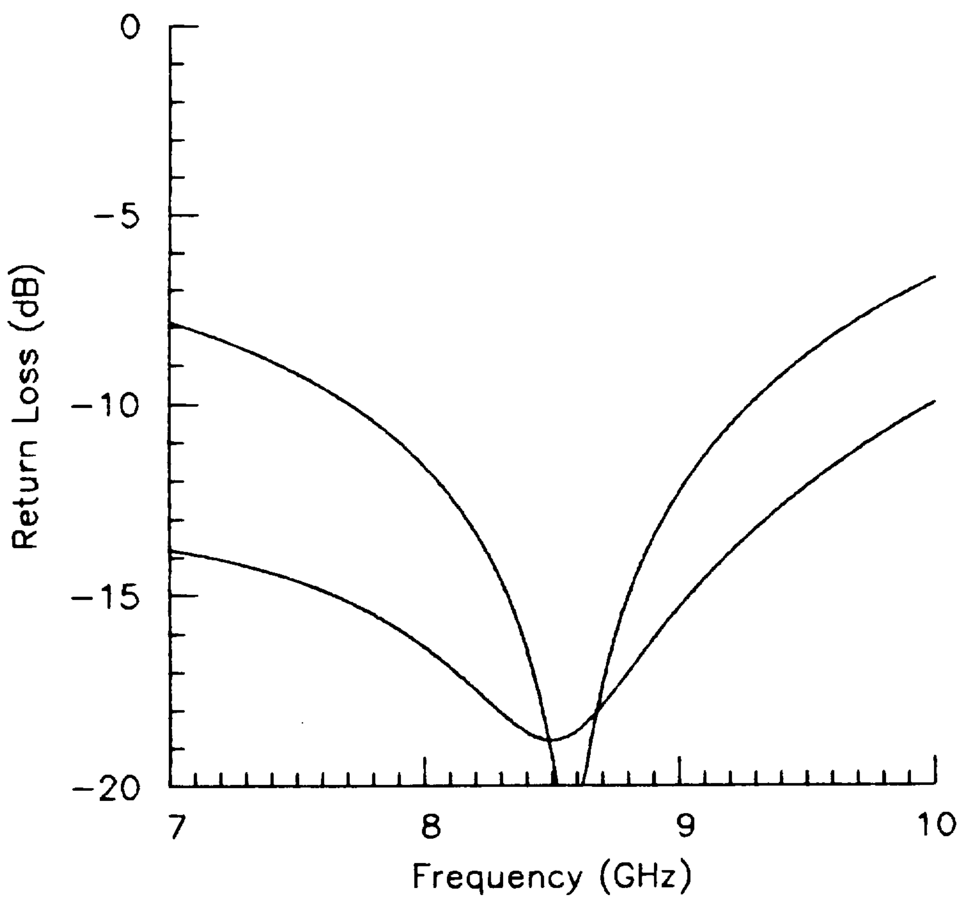

Figure 4.3-4) Predicted Input and Output Match of the 8.5 GHz 3 dB Power Splitter.

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5) MMIC FABRICATION

MMInc.'s GaAs wafer processing technology utilized in the fabrication of the dynamic dividers and related components is described in this section. MMInc.'s proprietary "Flash Annealing" process is described in section 5.1, and MMIC fabrication is described in section 5.2.

5.1) Flash Annealing

Ion implantation is a proven materials technology for GaAs FET and MMIC fabrication. Its advantages include simplicity of process, high uniformity and repeatability, and potential high throughput in volume production. The very thin active layer required by the present FETs is usually difficult to reproducibly prepare by other methods such as VPE (vapor phase epitaxy). The doping profile of ion implanted active layers, on the other hand, is determined by scattering at the atomic level, and is inherently predictable. Implantation into state-of-the-art bulk grown semi-insulating GaAs and high purity buffer layers has demonstrated excellent control of activation. This is hence a viable materials technology for accomplishing the program goals.

A severe limitation associated with conventional ion implantation technology is the requirement of annealing at temperatures of 850°C for periods of 30 minutes. For example, the diffusion length of Si in GaAs due to this annealing cycle is about 0.06 micron. This would certainly degrade the implant layer for the required devices. A method developed at MMInc., the Flash Annealing technique, reduces the dwell time at high temperature drastically, from typically 30 minutes to less than ten seconds. A typical temperature versus time profile of a flash annealing cycle is shown in Figure 5.1-1. A peak temperature of nearly 1000°C can be reached in about 5 seconds. Good activation has been obtained at peak temperatures as low as 800°C. Diffusion of impurities has been shown to be minimal. The quality of the annealed material is excellent as indicated by the high mobility. Low sheet resistivity n^+ layers have

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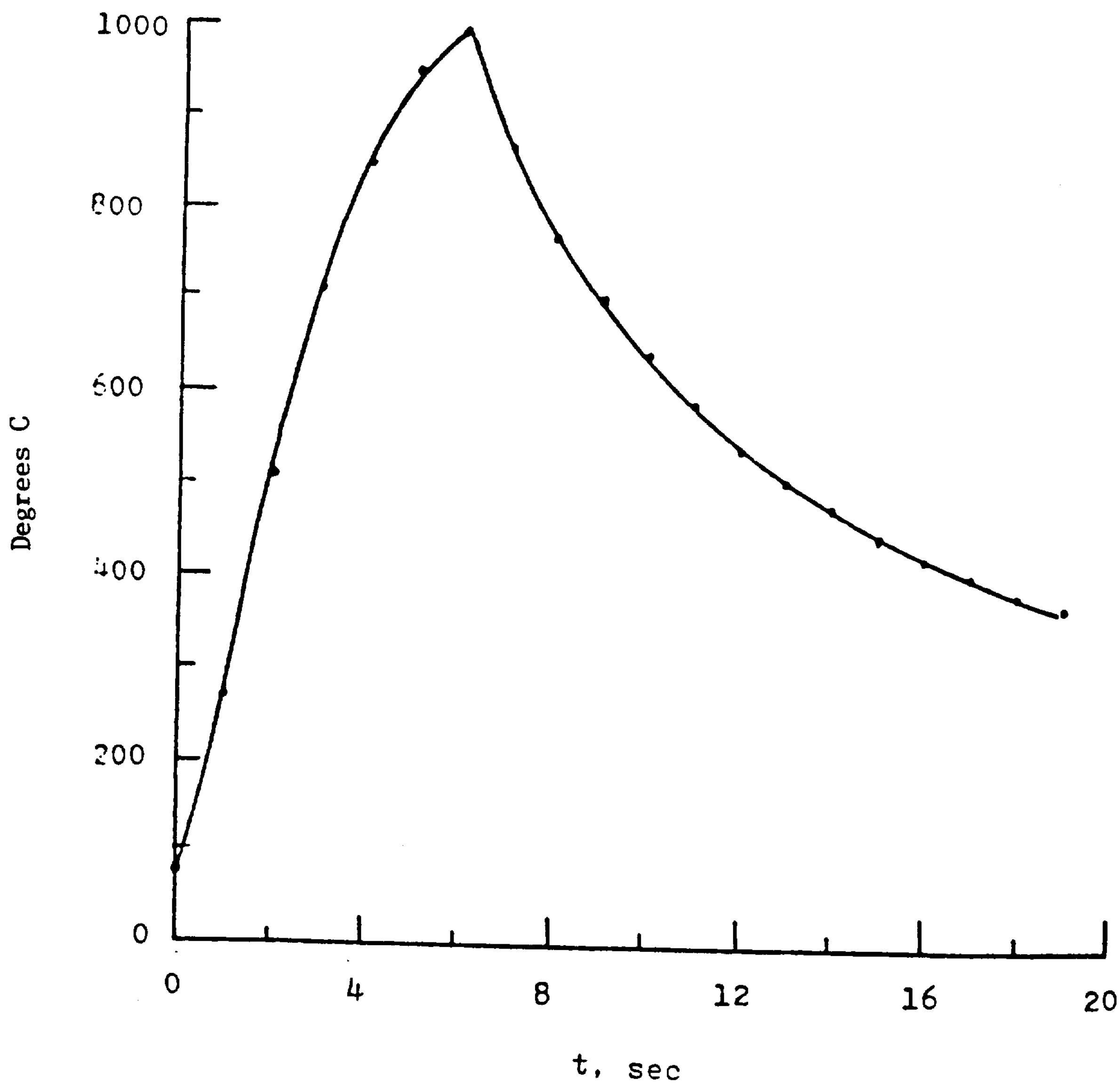

Figure 5.1-1) Typical Temperature vs. Time profile of a Flash Annealing Cycle.

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also been obtained using this method. Ti-W/Au Schottky barrier gates on n-GaAs which have been shown to exhibit insignificant degradation in diode characteristics at processing temperatures up to 900^{o}C are also compatible with the Flash Annealing process.

5.2) MMIC Processing

A summary of the processing sequence for the MMICs fabricated under this program is shown in Table 5.2-1. The processing starts with properly prepared GaAs substrates.

Resistors can be implemented by either ion implantation or metalization. In the former case the FET implant doses or separate implants can also be used if a selective implant scheme is employed. Ohmic contacts and electrode metalizations are then formed at the same time as the FETs, and hence no additional processing steps are required.

For low inductance on-chip grounding, substrate via connections are used. Via holes are formed after the wafers have been thinned to the final thickness for standard MMICs, and possibly as thin as 2 mils for discrete power FETs. The backside of the wafer is then metalized for ease of die-attach and low thermal resistance. This also forms the ground plane for the RF circuitry in MMICs. Individual chips are obtained following dicing.

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Table 5.2-1 STANDARD MMIC PROCESSING SEQUENCE

1.	Ion Implantation		1'.	Implant Mask
2.	Annealing	or	2'.	Ion Implantation
3.	Mesa Etch		3'.	Annealing

- - - - - - - - - -

4. Ohmic Contact
5. Gate
6. Overlay (First Layer) Metalization
7. Dielectric(s)
8. Additional Layer(s) Metalization
9. Wafer Thinning, Via Hole Etching, and Backside Metalization
10. Dicing

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6) 8.5 GHz COMPONENT CHARACTERIZATION

Due to the common processing parameters for the voltage controlled oscillator, the power splitter, and the regenerative divider circuit, all circuits on each wafer are suitable for testing. This is as planned since the chips will ultimately be part of a single, larger, MMIC. Therefore, each of the MMICs described in the preceding sections were individually mounted in the appropriate test fixturing, and were subsequently characterized to determine their RF performance characteristics. The results of these RF evaluations are presented in the following subsections.

6.1) 8.5 GHz Monolithic Dynamic Divide by Four

Following mounting and final verification of DC performance for a 2.0 by 1.5 millimeter dynamic divider chip, it was biased with 5 volts on the FET drain supply bus, and -0.8 volts on all three gate bias ports. The monolithic chip is intended to operate in this mode (a common bias voltage for all gate leads), however the gate bias lines were individually routed to external bonding pads for this initial design iteration in case adjustments and/or diagnostic tests became necessary. The gate bias voltage setting is critical, which is to be expected with the active load FETs used in this design.

The divider MMIC was then driven with a microwave sweeper, and the output signal was observed on a spectrum analyzer. With no RF input signal, the free running output oscillation frequency was measured at 2.057 GHz. This value is quite close to the predicted value. Next, the input signal level was adjusted to 0 dBm, and the input frequency was slowly swept between 8 and 9 GHz. A coherent (locked) output at one quarter of the input frequency was observed for input frequencies between 8.12 and 8.56 GHz, corresponding to output frequencies of 2.03 and 2.14 GHz respectively. Output power remained nearly constant at approximately -11 dBm. Harmonic and idler output signals were all

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observed to be at least 10 dB below the primary output signal, indicating that the loop and output filters are operating as desired.

Thus, this initial divider design covers the desired operating frequency of 8.415 GHz but is centered at a slightly lower frequency. Also, output power from the on-chip source follower buffer amplifier is somewhat lower than expected.

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6.2) 8.5 GHz Monolithic VCO

The 1.1 by 0.9 millimeter VCO chip was biased with -4 volts DC on both the V_{ss} and V_{tune} bias ports, resulting in a output signal level of approximately -10 dBm at 8.5 GHz as read on the spectrum analyzer. This signal was continuously tunable up to 8.8 GHz by adjusting the V_{tune} voltage, which effectively alters the gate capacitance of the oscillator FET and thus modifies the resonant frequency of the on-chip resonator. The resonator consists of the FET gate to source capacitance and a spiral inductor. A second chip, selected from the same wafer lot, produced an output signal level of approximately 0 dBm, however the output frequency in this case was tunable between approximately 8.0 and 8.4 GHz.

Both MMICs were then examined in detail with the aid of a microscope to ascertain why performance varied to this extent. It rapidly became obvious that the first result was invalid since a breakdown had occurred in one of the small tuning capacitors between the oscillator FET and the buffer FET. This malfunction had the effect of loading the oscillator FET, thereby reducing the output power, and pulling the operating frequency away from the resonator frequency. This hypothesis was verified by measurement of additional VCOs, which had performance characteristics virtually identical to the undamaged VCO. Therefore the operating frequency of this first iteration VCO design was slightly low, and the output power was lower than anticipated.

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6.3) 8.5 GHz Power Splitter

Due to the symmetry of the 3 dB power splitter, only half of the circuit must be characterized. Thus an MMIC was selected and subsequently mounted on a carrier similar to that utilized for the divider. The additional output port was terminated with a small 50 ohm chip resistor. Input return loss, output return loss, and insertion loss were then measured on a network analyzer. The results of these measurements are shown in Figures 6.3-1 through 6.3-3. Figure 6.3-1 and 6.3-2 are the measured input and output return loss, respectively, while Figure 6.3-3 shows the measured insertion loss. Note that the insertion loss curve includes the 3 dB loss due to the power split, and that all measurements include the fixture insertion loss of approximately 0.4 dB.

It is clear from this measured data that the initial divider design is operating as desired and covers the band of interest. However, it is also clear from the return loss curves that the center of the operating band is shifted to a lower than expected frequency.

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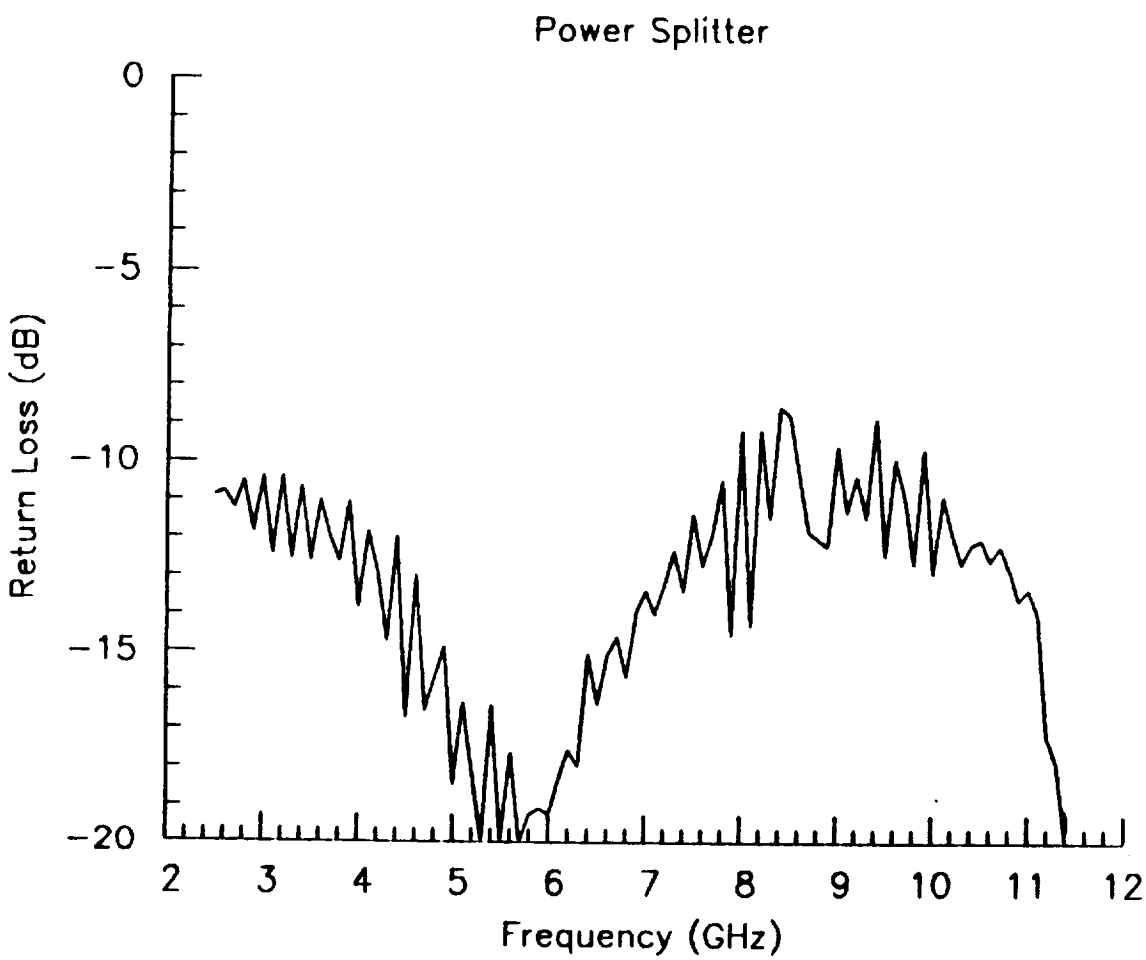

Figure 6.3-1) Measured Input Return Loss for the First Iteration Power Splitter.

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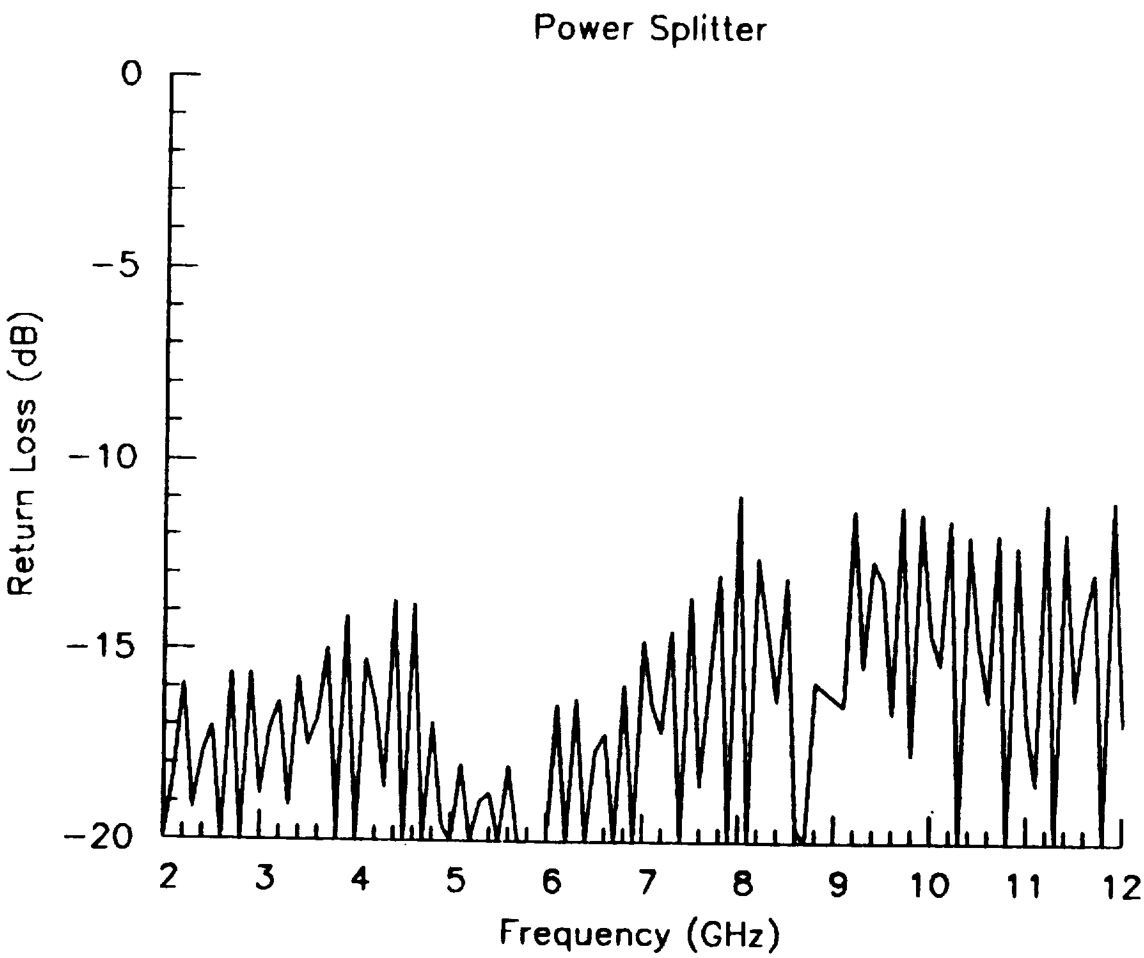

Figure 6.3-2) Measured Output Return Loss for the First Iteration Power Splitter.

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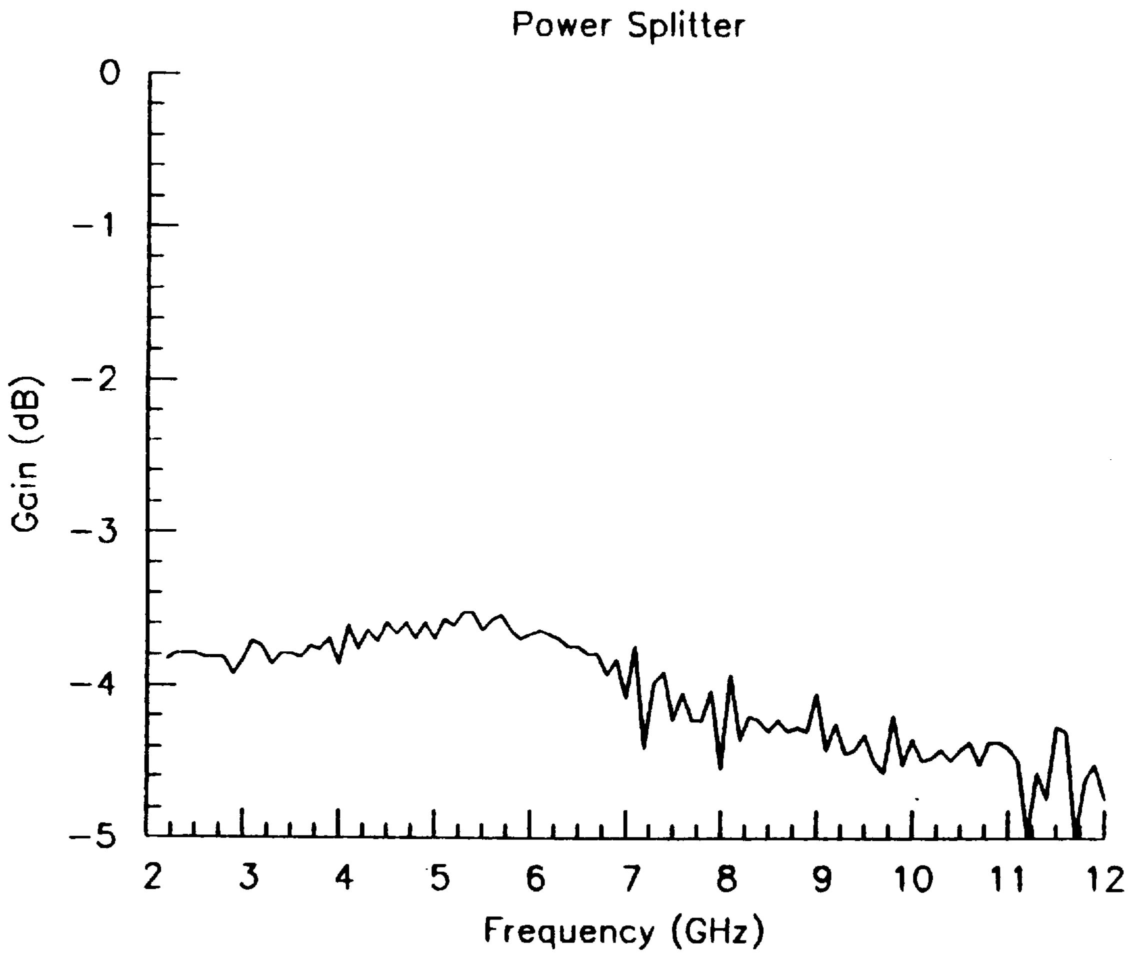

Figure 6.3-3) Measured Insertion Loss of the First Iteration Power Splitter, Including 3 dB Due to the Power Division.

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6.4) Measured Integrated Component Performance

To test the combination of the VCO and dynamic divider as a single "super component", each was mounted in a separate test fixture, individual performance was verified, and the two fixtures were then "integrated" with coaxial connectors. Although it is possible to provide a third RF port for this test fixturing, it was not utilized for these initial tests. Therefore a 3 dB attenuator was also inserted between the VCO and the divider to simulate the effect of the power splitter.

When mounted in the custom test fixture described above, the VCO/divider super component generated a coherent divide by four output signal over tuned VCO frequencies of 7.96 to 8.28 GHz, which corresponds to output frequencies from 1.99 to 2.07 GHz. This frequency band is slightly lower than the design value, which is as expected since the individual components operate at lower frequency. The bandwidth is also somewhat reduced since the operating band of the first iteration VCO and divider do no exactly coincide. As expected, output power was identical to that of the divider alone.

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7) 8.5 GHz DESIGN ITERATION

This section describes the second iteration design modifications which were performed for the "8 GHz" MMICs to correct the deficiencies identified as a result of characterizing the first iteration MMICs. Measured performance for these iterated designs is then presented at the end of this section, including performance as an integrated "super component".

7.1) Design Modifications

7.1.1) Regenerative Frequency Divider

As previously described, the operating band for the first iteration "8 GHz" divider covers from 8.12 and 8.56 GHz, corresponding to output frequencies of 2.03 and 2.14 GHz respectively. This band includes the desired operating frequency of 8.415 GHz but is centered at a slightly lower frequency. It has been determined that an adjustment in the length of the feedback delay line, combined with a minor adjustment in the size of the spiral inductors on the loop amplifiers, would center the operating band. More interesting, however, is the determination that similar changes can be utilized to lower the center frequency to 7.9656 GHz.

During a telephone conversation on December 19, 1988 between the program technical monitor, Dr. Narayan R. Mysoor, and Dr. Daniel R. Ch'en of MMInc., the specific design frequency for the "32 GHz" circuitry was identified as 31.86225 GHz. Therefore the divide by four output frequency is centered at 7.9656 GHz. Thus to test the "32 GHz" divider (described in a following section) in combination with the "8 GHz" divider, a lower operating band for the 8 GHz divider is necessary. The mask tool set drawing changes to accomplish this were therefore included on the second iteration mask tool set design along with those changes necessary to slightly raise the frequency of the "8.5 GHz" divider.

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Output power for the 8 GHz divider is nearly constant at approximately -11 dBm, which is lower than expected. The reason was traced to the bias resistor on the source follower output stage, and the cutoff frequency of the low pass output filter. Corrections to these circuit components were therefore also included in the second iteration mask tool set design.

A photograph of the revised monolithic GaAs 8.5 GHz dynamic divider MMIC is shown in Figure 7.1.1-1.

7.1.2) <u>Voltage Controlled Oscillator</u>

As previously described, the output power of the first iteration VCO design was lower than anticipated, and the operating frequency was slightly shifted downwards. These observed characteristics will be considered in sequence.

The lower than expected output power was traced to a bias resistor on the source follower output buffer which is larger than the original design value. It was thus straightforward to pre-distort the design value by the appropriate amount on the second iteration design to account for this effect.

One turn of the spiral tuning inductor on a the fully functional VCO was intentionally shorted to determine the "mechanical" tuning range, and the resulting MMIC exhibited an oscillation frequency above 9 GHz. This destructive modification of the VCO resonator clearly indicated that the frequency can easily be pulled over a wide range with a slight scaling of the inductance value. This experimental observation agrees well with the predicted range of negative impedance for this circuit as described previously for the initial circuit designs. It is not possible to exactly adjust this value via these external, necessarily crude, modifications, however the change was relatively straightforward at the mask tool set level. The modification was complicated, however, by the fact that varying the resistor to enhance

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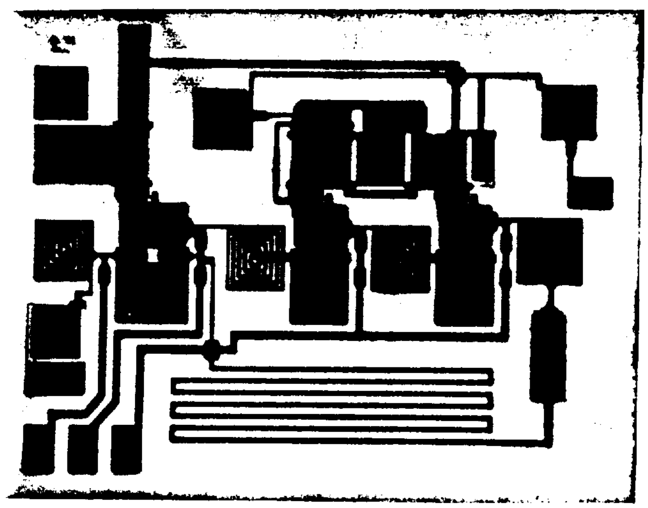

Figure 7.1.1-1) Photograph of the Revised Monolithic GaAs 8.5 GHz Dynamic Divider.

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output power is also predicted to raise the operating frequency. Therefore, some judgment was necessary to obtain the correct inductance value. However, since the measured tuning range is much larger than that required to lock the VCO to the desired operating frequency, it was not deemed necessary to exactly hit the desired frequency.

A photograph of the revised 8.5 GHz monolithic VCO is shown in Figure 7.1.2-1.

7.1.3) Power Splitter

It is clear from the previously described return loss curves that the center of the operating band for the power splitter is shifted to a lower than expected frequency. This effect has been traced to additional parasitic capacitances associated with the layout and the spiral inductors, and to somewhat different than projected inductance values. The center frequency for the second iteration design was therefore corrected by adjusting the size of the spiral inductors and the tuning capacitors.

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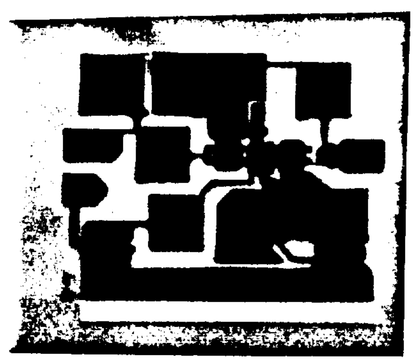

Figure 7.1.2-1) Photograph of the Revised 8.5 GHz Monolithic GaAs Voltage Controlled Oscillator.

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7.2) Component Measurements

Following a fabrication sequence identical to that utilized for the first iteration circuits, the iterated "8.5 GHz" designs described in section 7.1 were DC screened and mounted in the same test fixturing used for the initial testing. Measured performance of the new circuits is described in the following subsections, while performance of an integrated subsystem incorporating them is described in section 7.3.

7.2.1) Regenerative Frequency Divider

As originally predicted, the regenerative divider produced a coherent division by four over an input band which is somewhat sensitive to the input power level. This measured locking range, as a function of input power, is summarized in Figure 7.2.1-1 for a typical monolithic divider circuit biased with 4.0 volts on the drain and -1.0 volts on all gate bias lines. Note that for an input power of 7.5 dBm, a 1.3 GHz band from 8.1 to 9.4 GHz is covered, which reduces to a 0.4 GHz bandwidth covering 8.6 to 9 GHz at an the extremely low input power of -5 dBm.

When the bias conditions for this circuit are modified to 5.0 volts on the drain and -1.1 volts on all gates, the locking range is modified as shown in Figure 7.2.1-2. Bandwidth at 7.5 dBm input is virtually unchanged, however the center of the operating band is lowered to 8.4 GHz - nearly identical to deep space channel 14. Indeed, this channel is covered in both instances with input powers as low as 0 dBm.

To verify performance of the input matching network of the mixer portion of the dynamic divider, small signal input match was measured on an automatic network analyzer. The measurement is noisier than usual due to the free running oscillation which occurs under full bias, however it was deemed important to characterize this parameter under actual operating conditions. Measured input match under these conditions is shown in Figure 7.2.1-3, indicating that the match is centered at 7.7 GHz but is better than 2:1 as high as 8.5 GHz.

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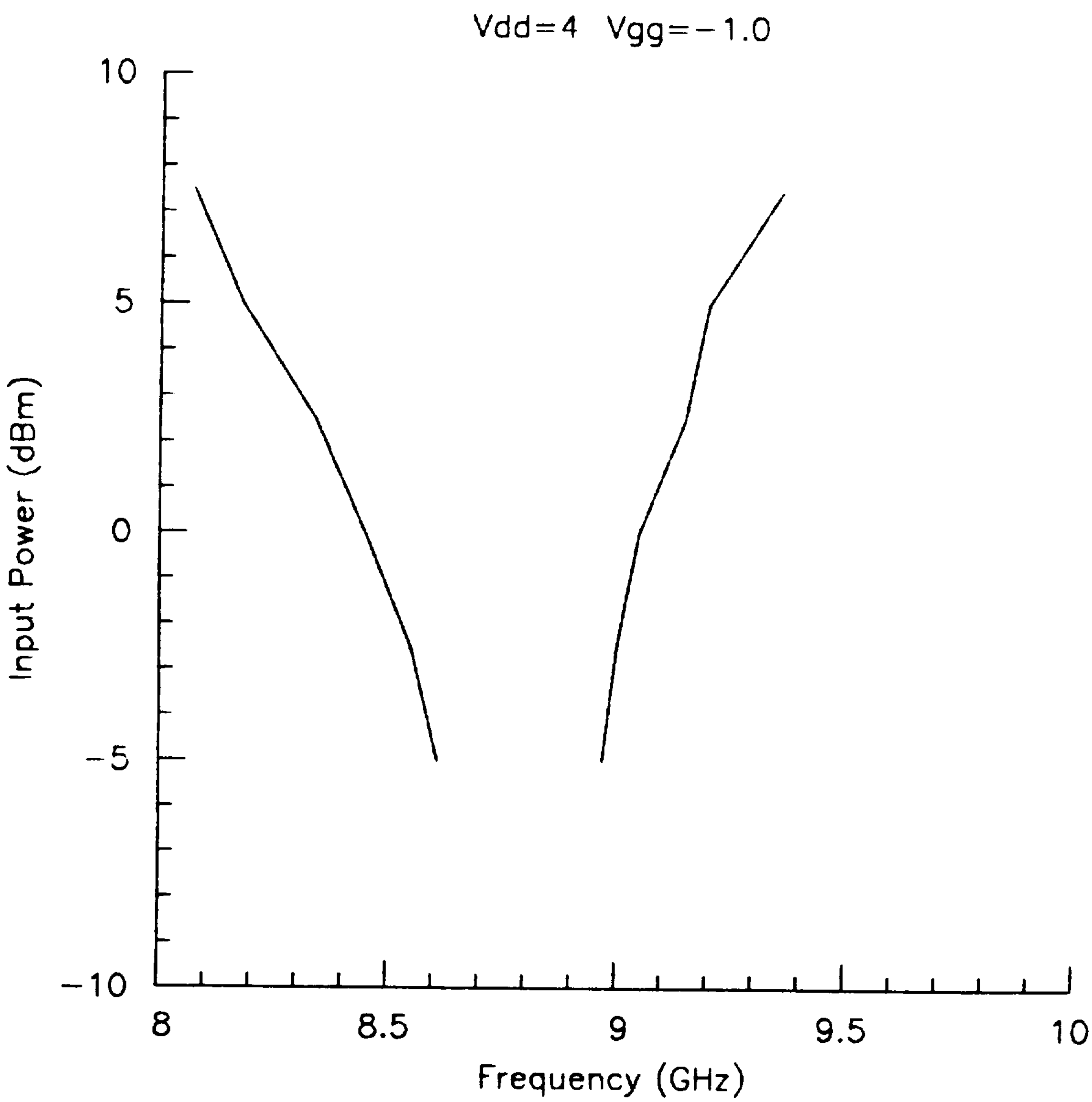

Figure 7.2.1-1) Measured Locking Range as a Function of Input Power for the 8.5 GHz Dynamic Divider. (V_{dd}=4.0, V_{gg}=-1.0)

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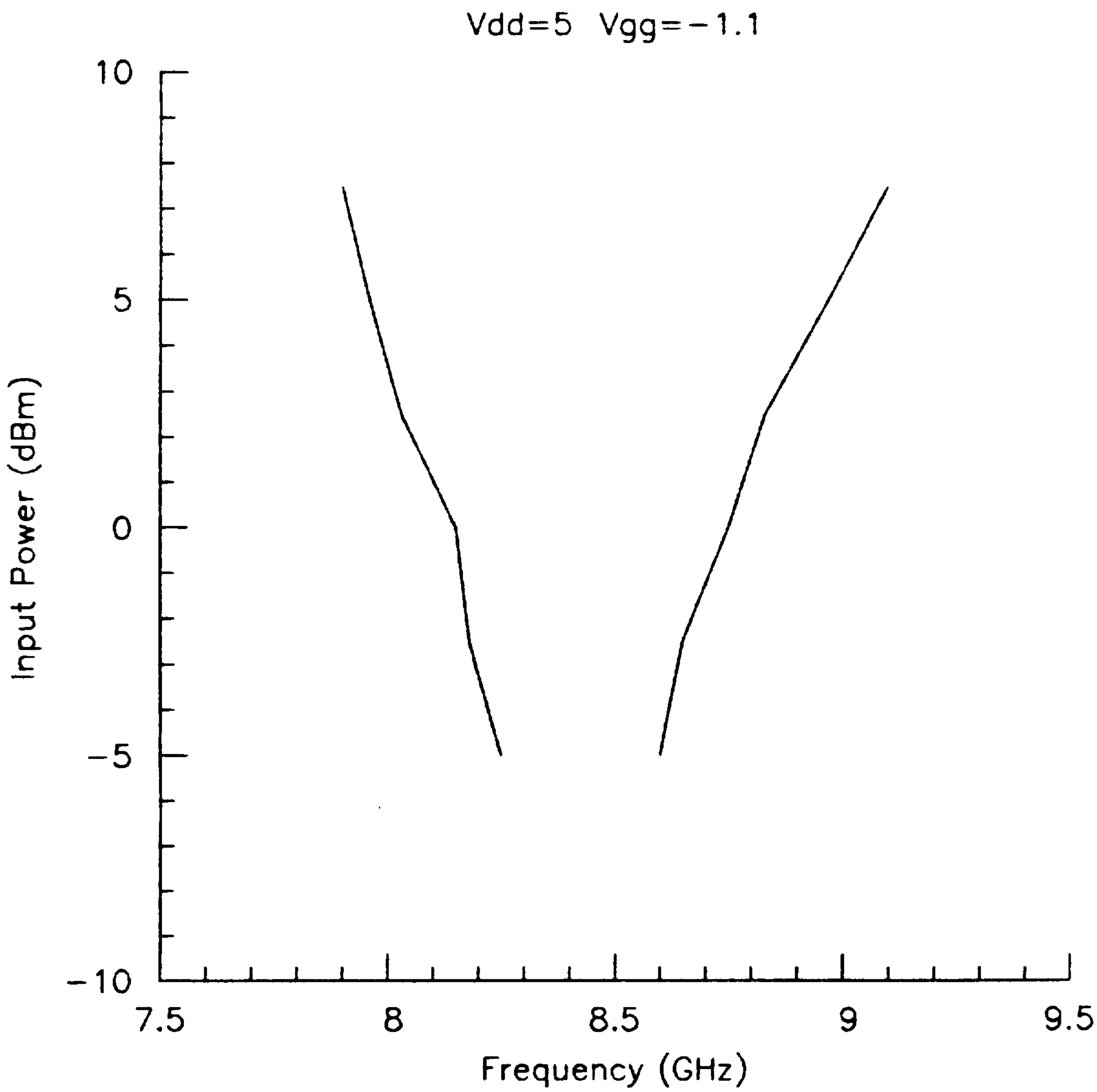

Figure 7.2.1-2) Measured Locking Range as a Function of Input Power for the 8.5 GHz Dynamic Divider. (V_{dd}=5.0, V_{gg}=-1.1)

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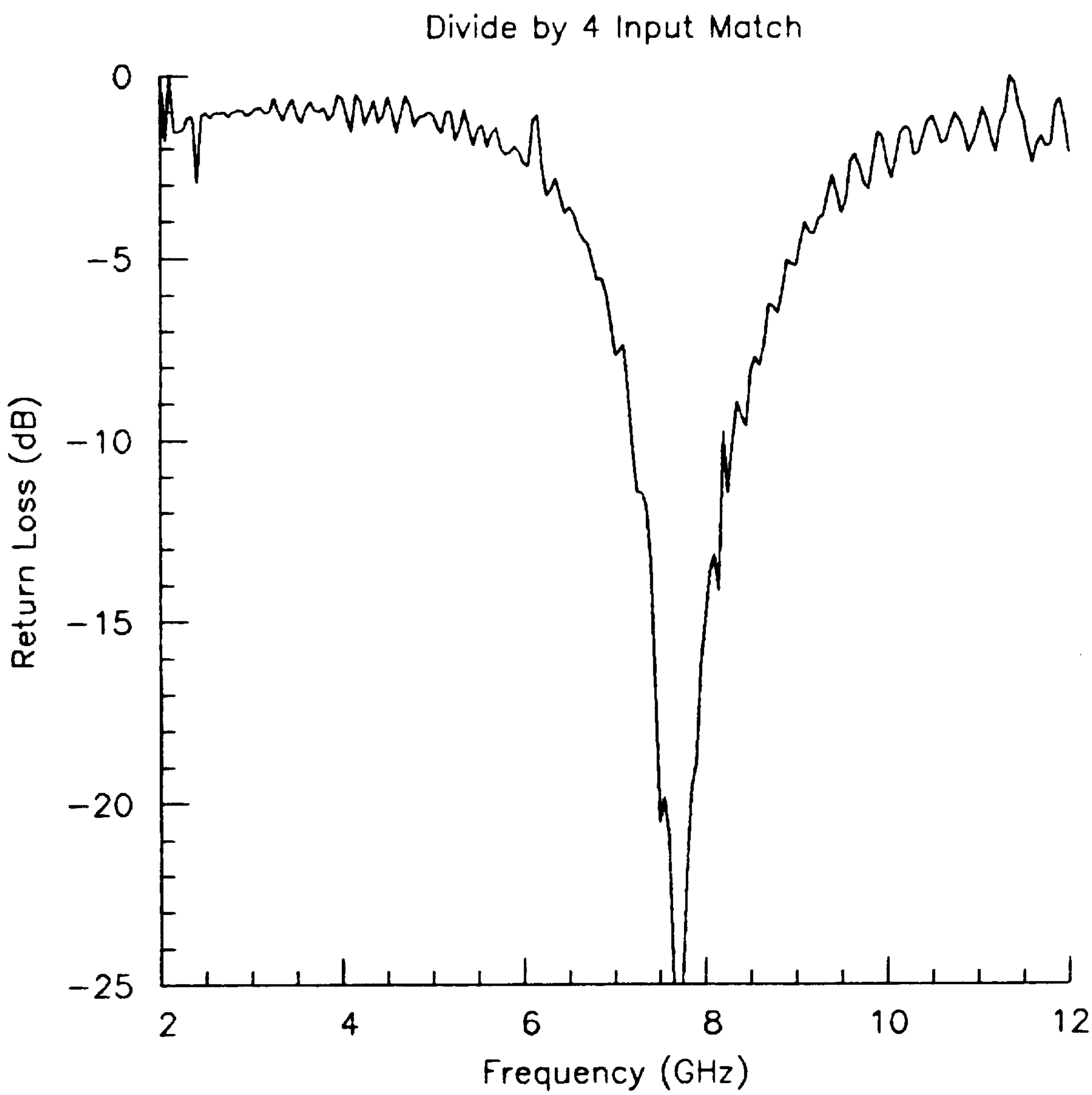

Figure 7.2.1-3) Measured Input Match of the 8.5 GHz Dynamic Divider.

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The output match was also characterized under actual operating conditions, and the results are summarized in Figure 7.2.1-4. Match is better than 1.5:1 up to 3 GHz, and rapidly deteriorates at the higher frequencies. This degradation is predicted, and actually desirable, since it is caused by the on-chip low pass filter which is utilized to reject the second and higher order harmonics of the nominally 2.125 GHz output signal. It indicates that a large degree of suppression has been obtained, especially at 6 GHz and above. Measurements were not made below 2 GHz, which was the lower operating edge for the particular network analyzer system utilized, however since the output filter is a low pass structure and the source follower tap is DC connected, output match at the lower frequencies will be dominated by the external DC blocking capacitor.

7.2.2) Voltage Controlled Oscillator

With the modifications described above, the newly fabricated VCOs produced an output power of +5 dBm, however the output frequency was not increased to the full extent anticipated. These performance results are summarized in Figure 7.2.2-1, which shows the measured output frequency vs. tuning voltage, and Figure 7.2.2-2, which shows the measured output power vs. tuning voltage.

It was determined that a single turn of the tuning spiral inductor could be reliably shorted with a very small drop of silver epoxy to shift the frequency to the desired operating band. This modification repeatedly moved the output frequency such that deep space channel 14 was included in the operating band. Output power was only slightly degraded by this modification. Measured tuning range and output power for this case are shown in Figures 7.2.2-3 and 7.2.2-4 respectively.

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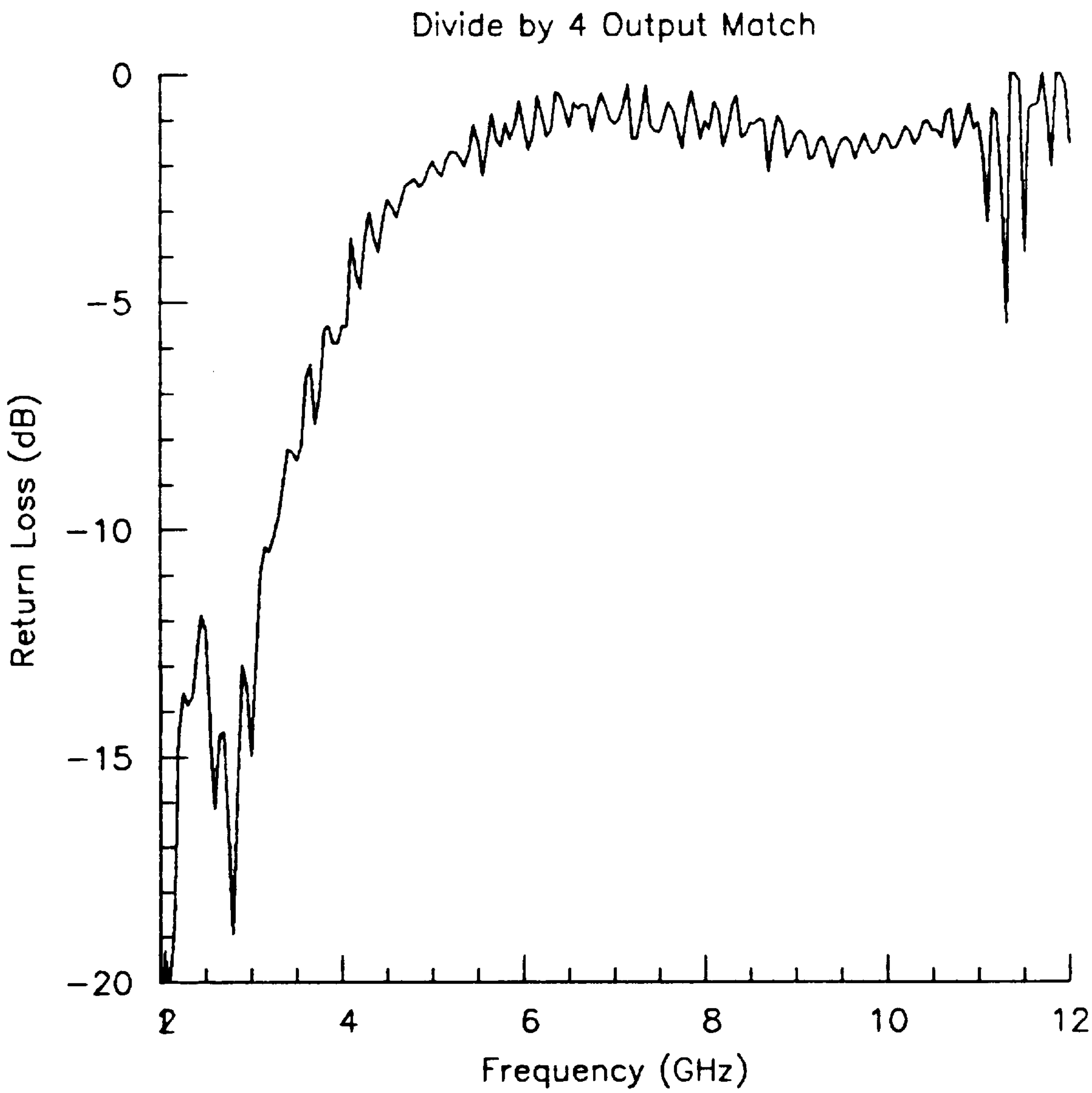

Figure 7.2.1-4) Measured Output Match of the 8.5 GHz Dynamic Divider.

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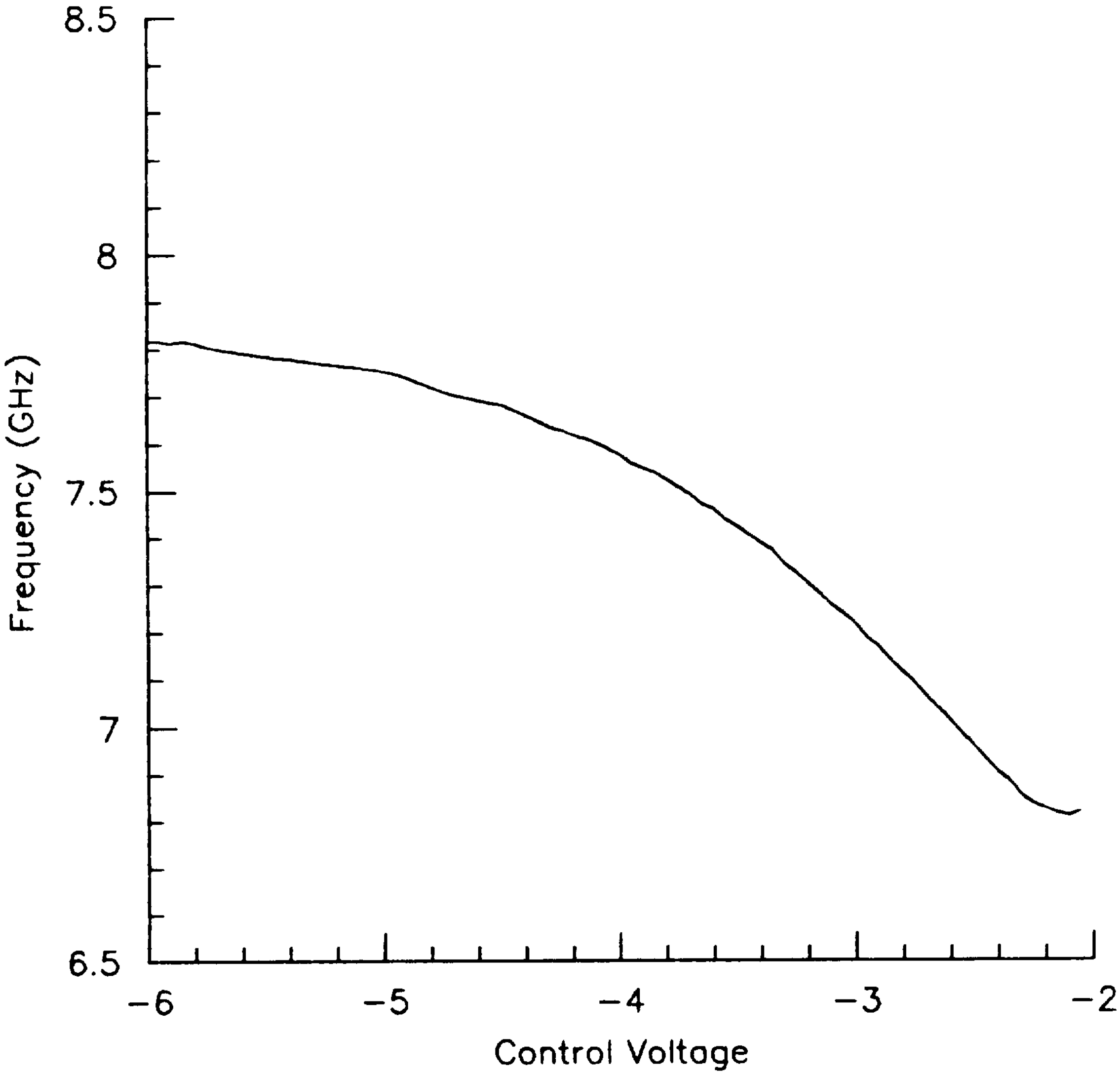

Figure 7.2.2-1) Measured Frequency vs. Control Voltage for the Monolithic GaAs VCO.

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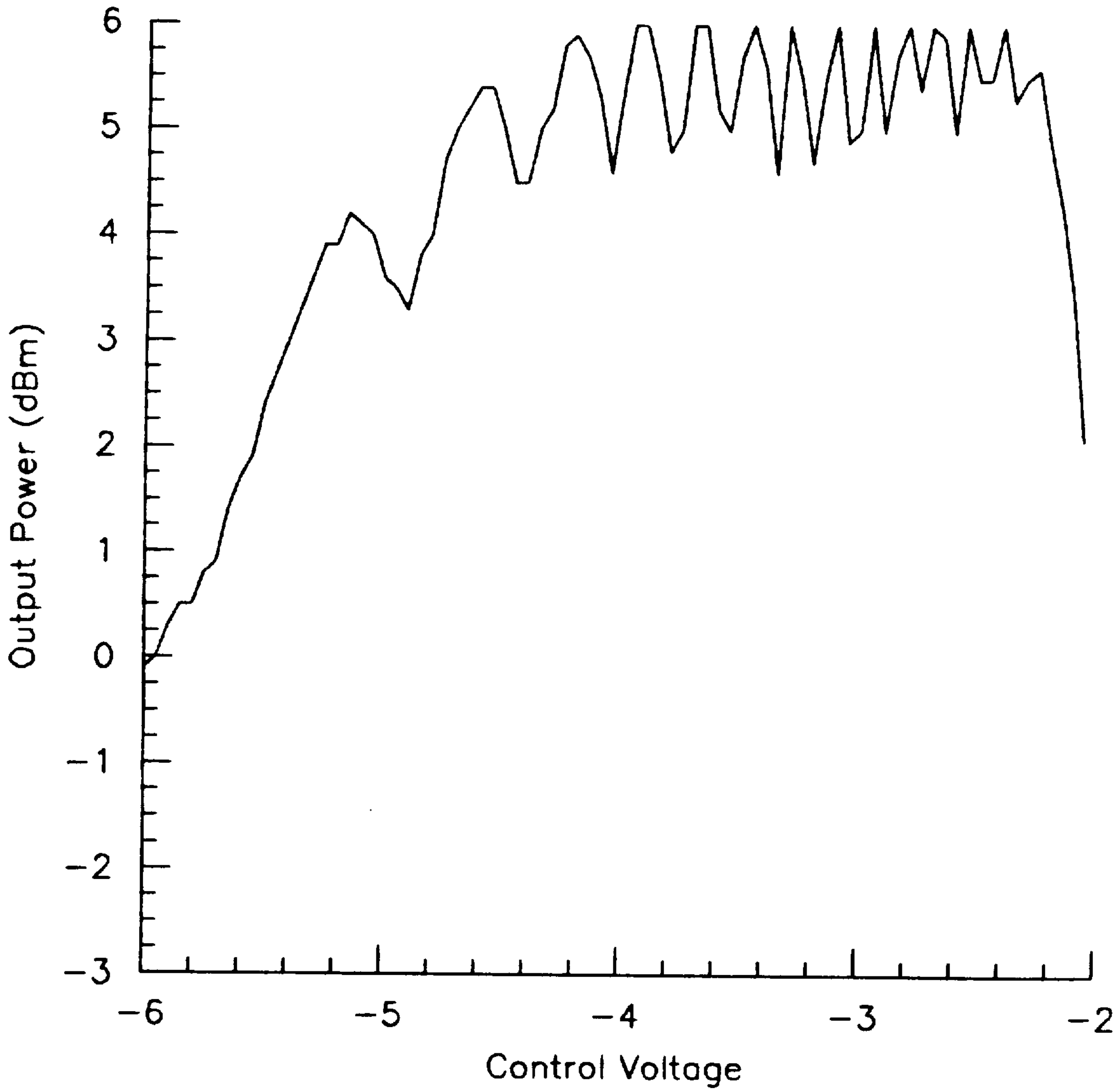

Figure 7.2.2-2) Measured Output Power vs. Control Voltage for the Monolithic GaAs VCO.

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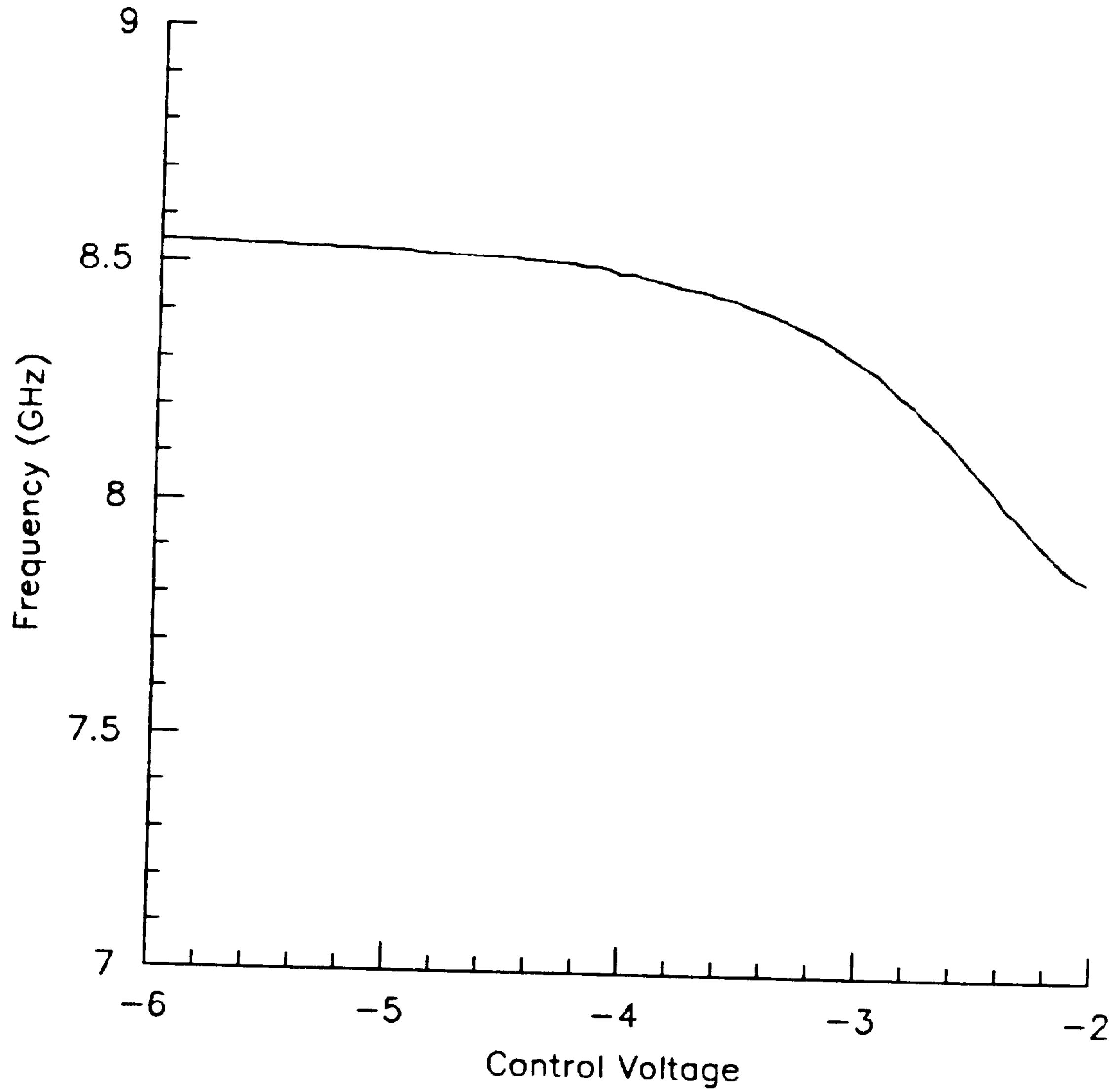

Figure 7.2.2-3) Measured Frequency vs. Control Voltage for the Modified Monolithic GaAs VCO.

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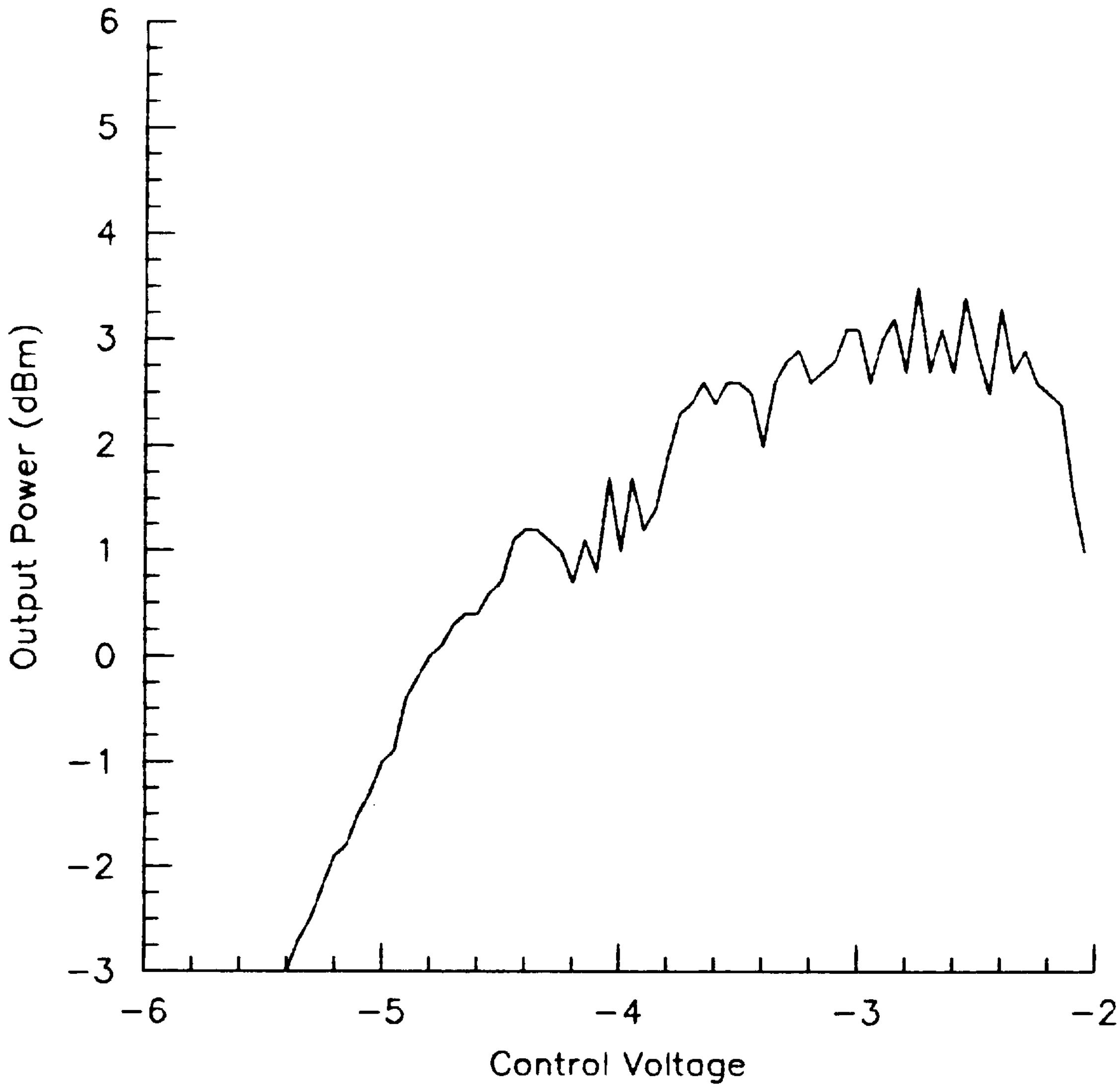

Figure 7.2.2-4) Measured Output Power vs. Control Voltage for the Modified Monolithic GaAs VCO.

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7.2.3) Power Splitter

The iterated power splitter was mounted in the same test fixture utilized for the initial measurements, including the 50 ohm termination resistor on the second (physically and electrically symmetrical) output port. Measured input and output return loss under these conditions are shown in Figure 7.2.3-1. It is clearly evident from this figure that the center frequency has been shifted to 8.5 GHz as desired. The input match is better than 2:1 from 5 to 11 GHz, while the output match is better than 1.5:1 over the same band. The measured insertion loss, including the 3 dB loss due to the power split, is shown in Figure 7.2.3-2. Resistive losses, as indicated from this figure, are thus in the 0.5 to 1 dB range in the operating band. Approximately half of this resistive loss is due to losses in the test fixture and carrier, which have not been deducted from the measured data shown in Figure 7.2.3-2.

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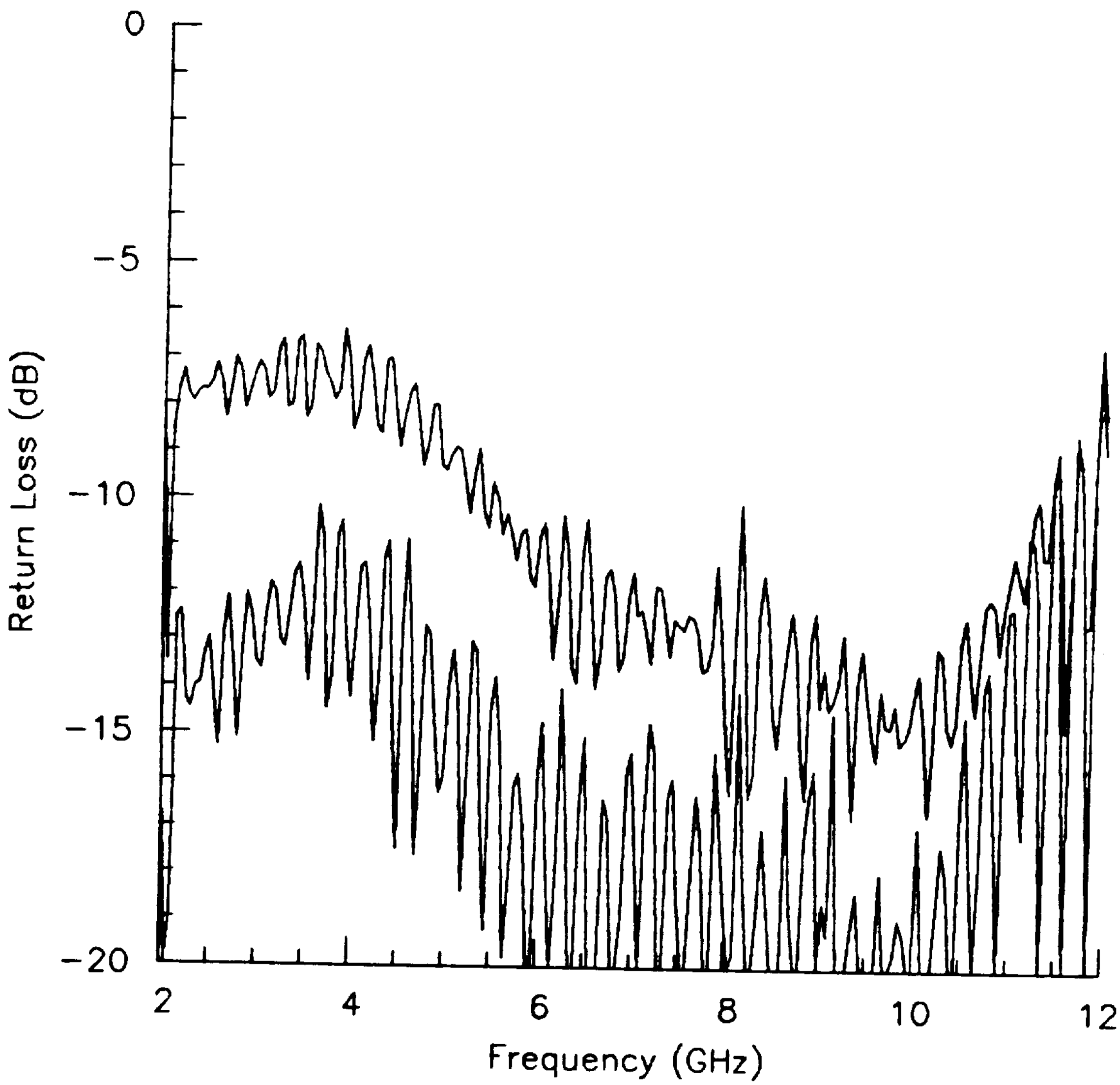

Figure 7.2.3-1) Measured Input and Output Match of the 8.5 GHz Power Splitter.

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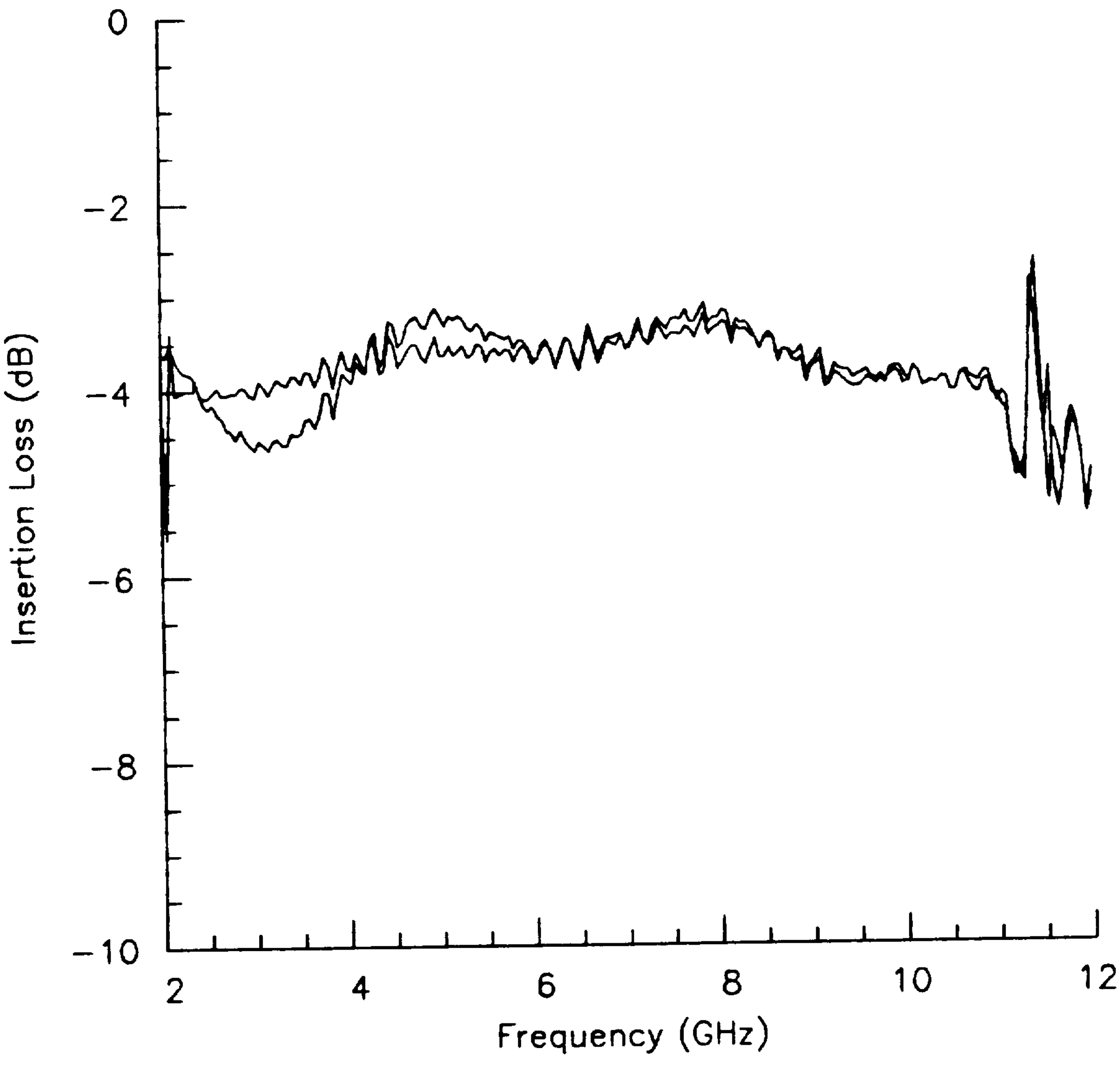

Figure 7.2.3-2) Measured Insertion Loss of the 8.5 GHz Power Splitter, Including the 3 dB Loss Due to the Power Split.

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7.3) Measured Integrated Component Performance

It is clear from the data presented in section 7.2 that all three components are functioning as required to construct an integrated 8.5 GHz VCO with a coherent output reference signal at 2.125 GHz. Therefore three MMICs were selected and mounted on a single test carrier for characterization as an integrated "super component".

After additional bypass capacitance (0.01 uF) was soldered to selected test fixture bias pins to suppress a spurious oscillation at 14 MHz, functionality of this component was easily verified by manually tuning the control voltage of the VCO and observing both the 8.5 and 2.125 GHz output signals. Therefore it was determined that this unit could be characterized as the key part of a phase locked loop.

For the phase locking experiments, an EIP 575 frequency locking counter provided the remaining, low frequency, portion of the phase locked loop. The course and phase lock control lines of the locking counter were combined in an operational amplifier summing network, which also provided the necessary DC offset voltage. The schematic of this interface network is shown in Figure 7.3.-1. The other three fixed DC bias voltages were obtained from standard laboratory power supplies.

Without adjusting any bias voltages, other than the VCO gate voltage controlled by the locking counter, the "super component" was successfully locked to a variety of frequencies via the counter's keyboard. For this experiment, the "8.5 GHz" output was routed to a spectrum analyzer and the "2.125 GHz" reference output was routed to the locking counter for phase locking. A sequence of photographs of the spectrum analyzer screen as the lock frequency is incremented across the band is shown in Figure 7.3-2. From these photographs it is clear that the divider performs as intended for phase locked loop applications. Note also that deep space channel 14 is included in the sequence of photographs.

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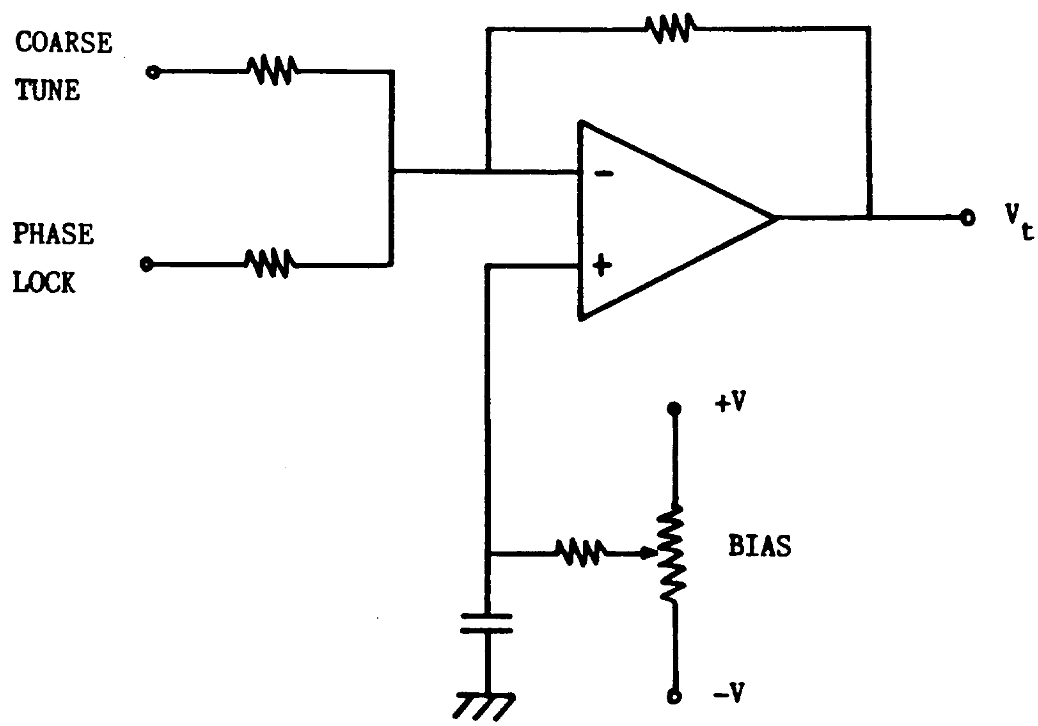

Figure 7.3-1) Schematic Diagram of the Operational Amplifier Summing and Bias Interface Network Between the Locking Counter and the Monolithic GaAs VCO.

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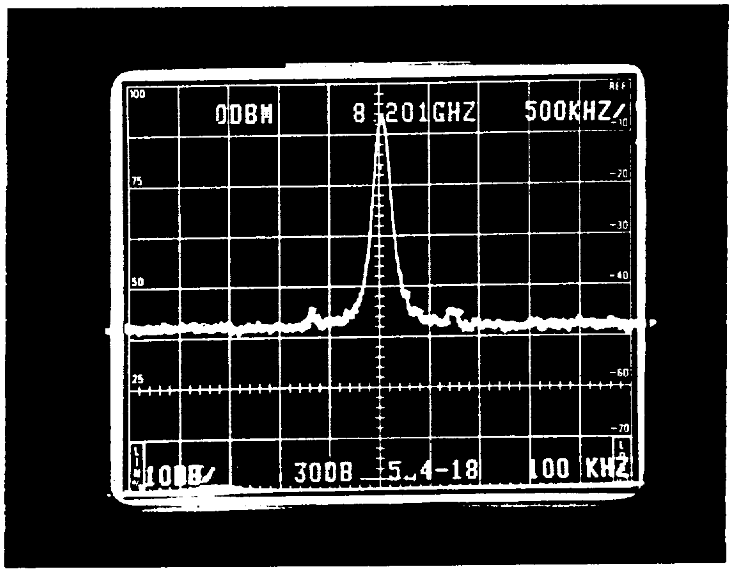

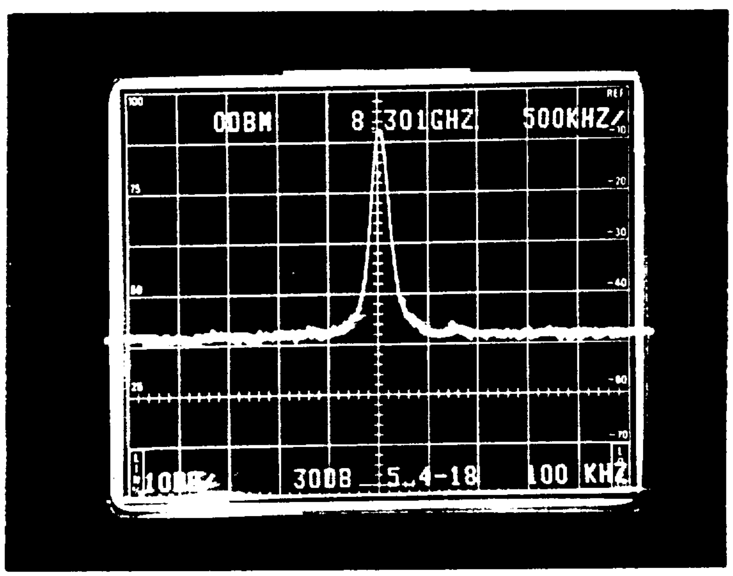

Figure 7.3-2) Sequence of Spectrum Analyzer Photographs Demonstrating Phase Locking of the Integrated GaAs VCO/Power Splitter/Dynamic Divider.

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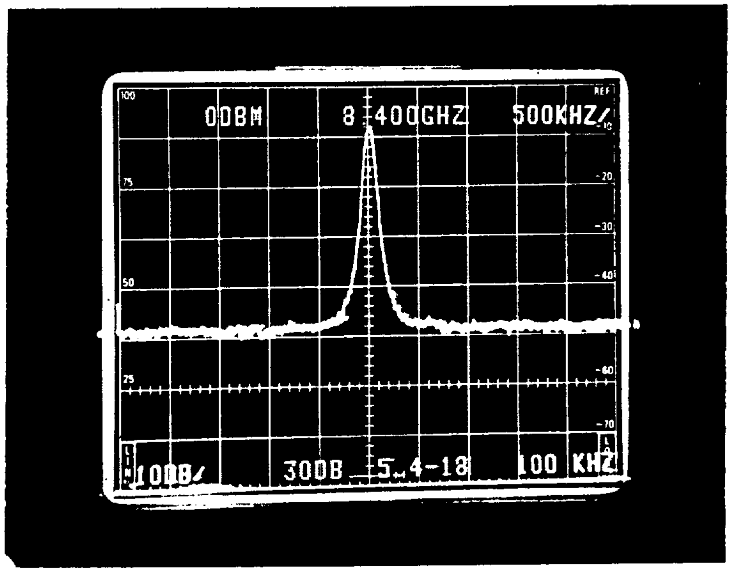

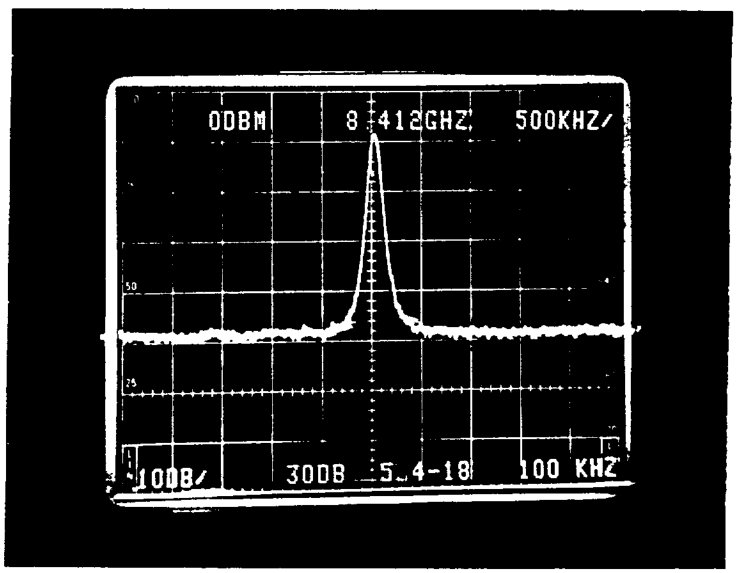

Figure 7.3-2) Sequence of Spectrum Analyzer Photographs Demonstrating Phase Locking of the Integrated GaAs VCO/Power Splitter/Dynamic Divider.

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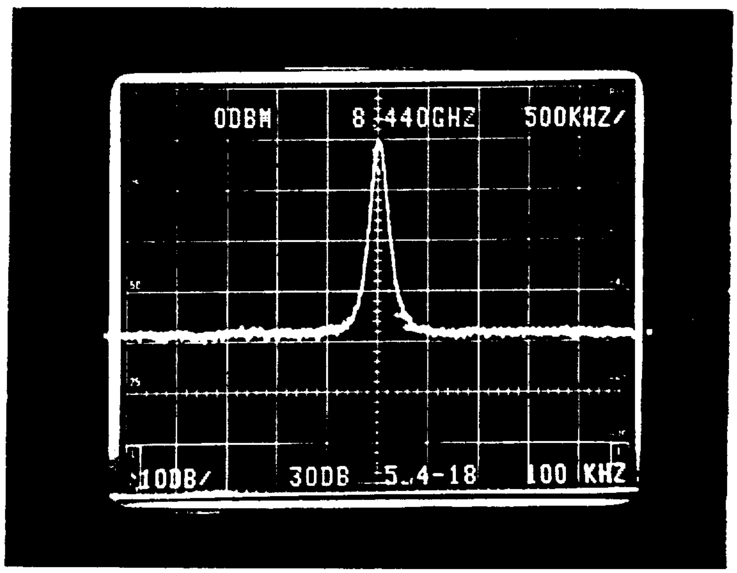

Figure 7.3-2) Sequence of Spectrum Analyzer Photographs Demonstrating Phase Locking of the Integrated GaAs VCO/Power Splitter/Dynamic Divider.

Although the integrated supercomponent described above consists of four individual MMIC chips mounted next to each other on a carrier, they were in fact all fabricated at the same time on the same wafer. Furthermore yields are high enough that if integrated as a single monolithic component, fully functional GaAs MMIC sources with integral dividers would be obtained. Figure 7.3-3 shows a pen plot of this fully lockable GaAs MMIC source with integral divider.

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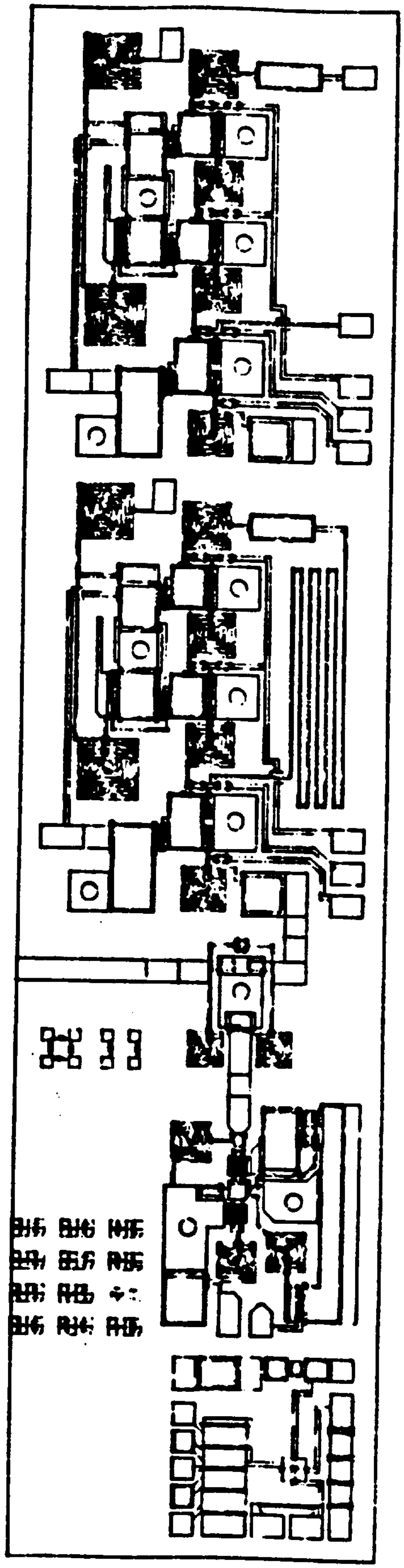

Figure 7.3-3) Layout of the Fully Integrated 8.5 GHz Source with on-chip Dynamic Divider.

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8) 32 GHz DYNAMIC DIVIDER

As determined by the technical monitor, the actual operating frequency of the "32 GHz" divider was identified as 31.86225 GHz. Due to the higher operating frequency, the FETs utilized in this circuit design requires shorter gate lengths than the 0.75 micron gates utilized for the 8 GHz circuitry. It is important to note, however, that the active devices are not required to operate at 32 GHz. The highest frequency where gain is required is the 3/4 idler frequency of 24 GHz. Thus FETs with a nominal gate length of 0.6 microns will suffice for the current application. Although MMInc. could fabricate 0.5 micron devices if necessary, yield considerations clearly favor the longer gate length. The mixing FET in the regenerative loop circuit must, of course, operate at 32 GHz, however this constraint is not as severe as a requirement for gain. Although the conversion loss of this mixing device will be somewhat higher with this approach, the loss can be compensated by additional gain at the lower, and more manageable, frequencies of 8 and 24 GHz.

8.1) Monolithic Circuit Design

In many respects, the design approach used for the 32 GHz divider follows the proven 8 GHz design. However, the predicted delay through the three stage loop amplifier is already beyond the necessary 360 degrees, therefore phase advance circuits are utilized in place of the delay line in the 8 GHz circuitry. The phase advance is implemented as high pass series capacitor-shunt inductor-series capacitor networks, which also provide a convenient DC blocking function. Their phase shift linearity over frequency is, however, quite different than the delay line unless an inordinate number of T-sections is constructed. Therefore predicted percentage bandwidth will be less than for the 8.5 GHz designs.

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A completely new mask tool set was required for this new 32 GHz divider design. Included on this mask tool set were the 32 GHz divider, circuit structures for test and evaluation, and all necessary process monitoring structures and devices. A schematic of the new 32 GHz monolithic dynamic divider circuit is shown in Figure 8.1-1, and a photograph of the completed MMIC chip is shown in Figure 8.1-2.

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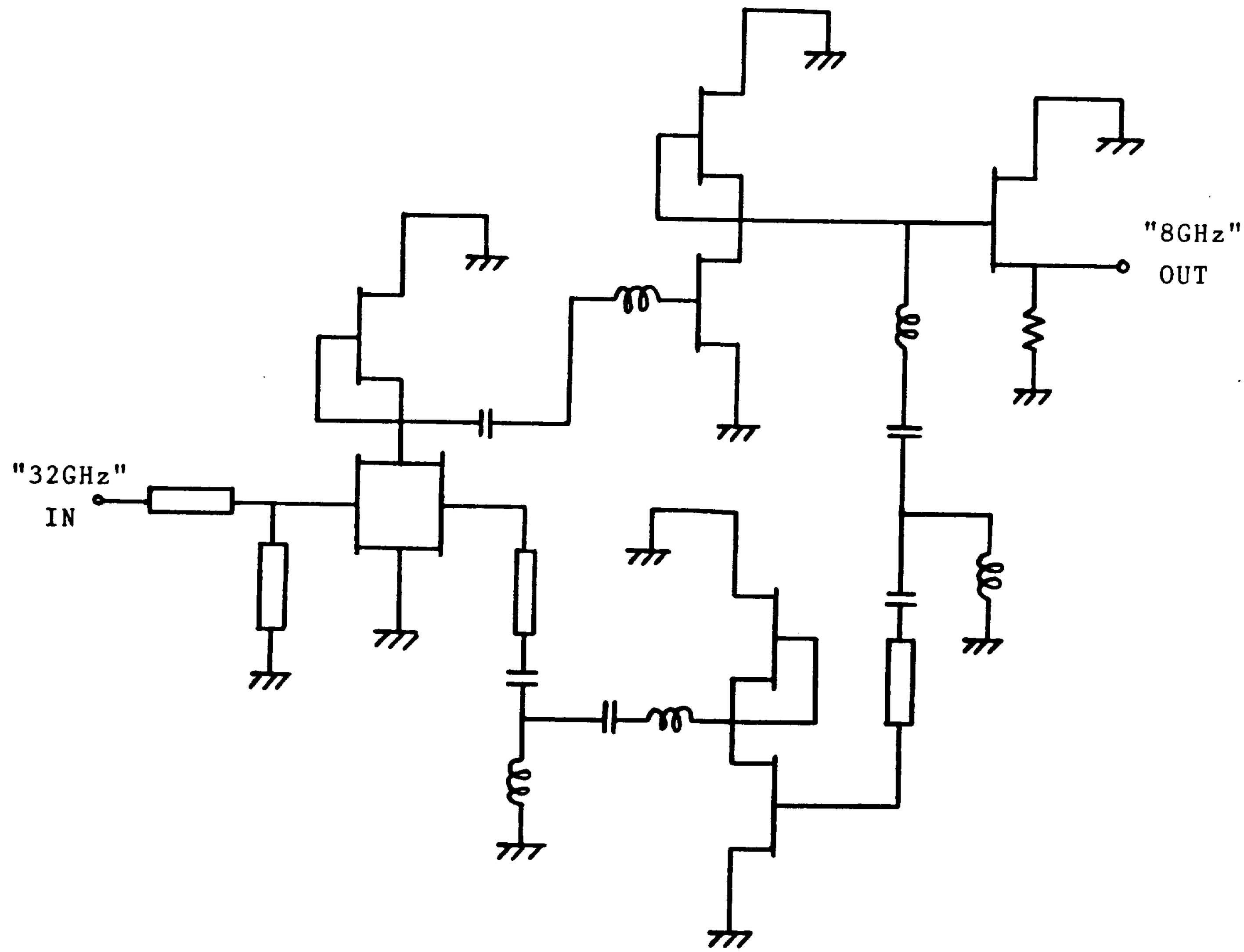

Figure 8.1-1) Schematic Diagram of the 32 GHz Quarter Frequency Dynamic Divider.

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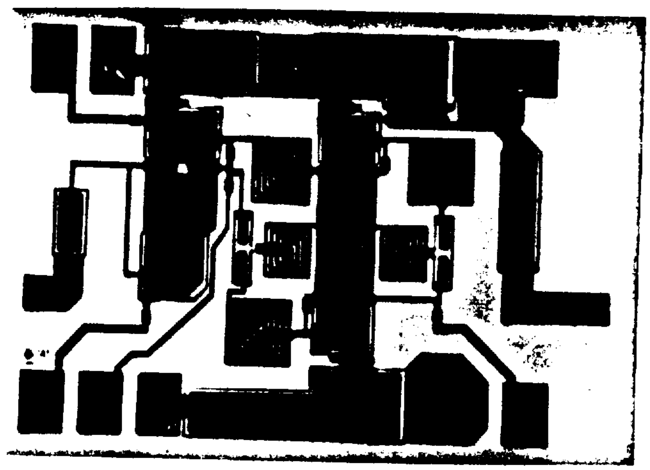

Figure 8.1-2) Photograph of the Monolithic GaAs 32 GHz Frequency Divider.

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8.2) Predicted Performance

Key to operation of the 32 GHz divider is the phase advance network which corrects for the excessive delay of the three stage loop amplifier at 32 GHz. The predicted phase shift of this network is shown in Figure 8.2-1. The phase shift at 32 GHz is the exact amount predicted to compensate for the loop amplifier, however it is far from "linear phase" as a more traditional delay line would be. A closer approximation to linear phase could be obtained from a multiple section high pass network, however additional modeling inaccuracies make use of such complex networks questionable at millimeter-wave frequencies.

With this network in place, the free running oscillation frequency is predicted to be 31.8 GHz, and under RF drive the predicted lock-in range covers from approximately 31.5 to 32.0 GHz with an input signal level of 10 dBm. The exact locking range is difficult to determine with MMInc.'s large signal analysis program, MMIC-SPICE, due to the long execution times and the circuits sensitivity to operating point variations.

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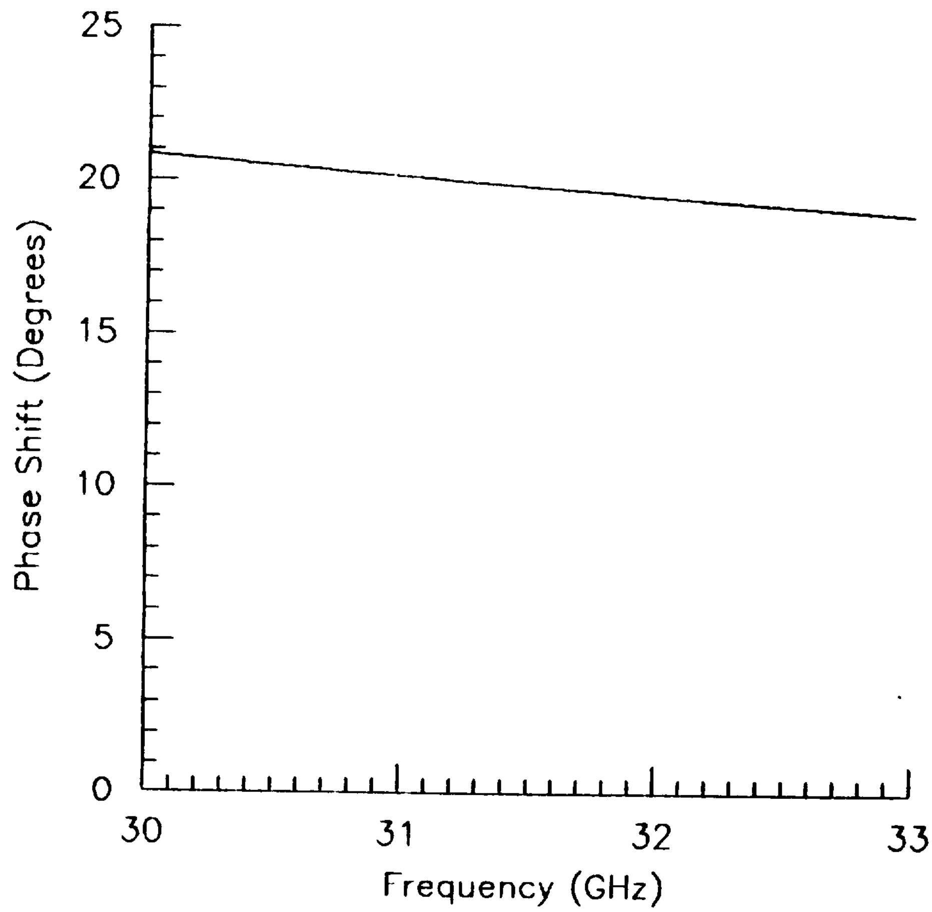

Figure 8.2-1) Predicted Phase Shift of the 32 GHz Phase Advance Circuit

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8.3) Measured Performance

For characterization, the 32 GHz dynamic divider was mounted in a suitable test carrier, and DC operation was verified. After determining the exact gate bias requirements, the MMIC demonstrated a free running loop frequency of 6.08 GHz rather than the design value of 7.9 GHz. Before attempting to adjust the loop frequency to the desired value, a 24.3 GHz input signal was applied to verify that a coherent output frequency at one quarter of the input signal was produced by this circuit.

Since a coherent quarter frequency was obtained, the divider was tested as part of a phase locked loop. The 24 GHz signal generator was directly controlled by the locking counter, and its output was routed to the dynamic divider. The divider output was routed to the input of the locking counter as well as to a spectrum analyzer for observation. Figure 8.3-1 shows a spectrum analyzer photograph of the locked 6 GHz output, clearly demonstrating that the circuit operates as intended except for the lower than expected operating band. Output power is also much lower than anticipated.

Detailed computer analysis and destructive characterization have indicated that the phase shift around the loop is not yet optimum for this first iteration 32 GHz circuit. However, unlike the 8.5 GHz circuitry, loop gain is also a function of phase shift due to the relatively high cut off frequency of the high pass networks. The latter is necessary to obtain significant phase advance, resulting in a large interaction between loop gain and phase shift. The main cause of this difference between predicted and measured performance is believed to be due to inadequacies in the spiral inductor model at millimeter-wave frequencies. By adjusting the cut-off frequency of the high-pass phase advance network, and possibly including a second phase advance network to reduce sensitivity to processing variations, it is clear that the 32 GHz divider could become functional with a second design iteration. Program constraints did not allow implementation this iteration.

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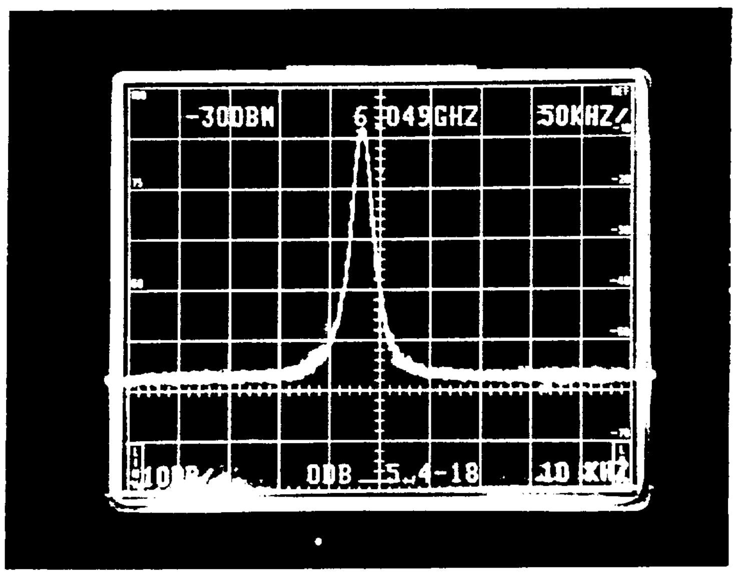

Figure 8.3-1) Spectrum Analyzer Photograph of a Locked Quarter Frequency Output Signal.

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9) CONCLUSIONS AND RECOMMENDATIONS

Proof of concept for MMInc.'s monolithic phase lockable source technology has been clearly demonstrated by the design, characterization, integration, and delivery of a deep space channel 14 GaAs VCO with coherent fourth sub-harmonic output. This integrated component operated over the 8.2 to 8.44 GHz band, and could be easily re-optimized for other similar applications. Proof of concept for operation into the millimeter-wave bands has also been demonstrated by design, characterization, and delivery of the key component of a similar subsystem - the monolithic GaAs divider chain. The first stage of this chain produced a coherent fourth sub-harmonic output over an input frequency band of 24.08 to 24.80 GHz.

In addition to obvious size and weight advantages inherent in GaAs MMIC technology, a significant benefit of these devices to NASA is increased longevity of deep space probes and satellites due to improved reliability and reduced prime power requirements.

Based on the demonstrated performance of these unique devices, it is recommended that a specific application be identified in conjunction with NASA/JPL, and that a fully integrated subsystem consisting of a VCO, power splitter, divider chain, reference oscillator, and phase locked loop be implemented. Maximum utilization of GaAs MMIC technology for the microwave and/or millimeter-wave circuits combined with silicon IC technology where its performance is proven will ultimately lead to a high performance, high reliability, small size and weight system ideally suited to NASA spaceborne applications.

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10) APPENDIX - HARDWARE DELIVERABLES

This appendix describes the hardware delivered to NASA for engineering data correlation per the contract data requirements list. A photograph of the items delivered is shown in Figure 10-1.

10.1) 8.5 GHz VCO with Integral Divider

As described in the body of this report, the monolithic GaAs 8.5 GHz VCO, the power splitter, and the 8.5 GHz dynamic divider were integrated on a single test carrier and mounted in a test fixture for evaluation as an integrated component. The pin out configuration of this component is as shown in Figure 10.1-1. Bias conditions for the test results, presented in Table 10-1, were:

V_s = 5.0 Volts @ 45 milliamps
V_t = -3.0 to -5.6 Volts (Controlled by phase locking circuitry)
V_d = 4.5 Volts @ 80 milliamps
V_g = -1.1 Volts

V_t and V_g consume just microamps.

The operating band can be modified to some extent by adjusting V_d, however this voltage should not exceed the operating limits summarized in Table 10.1-2.

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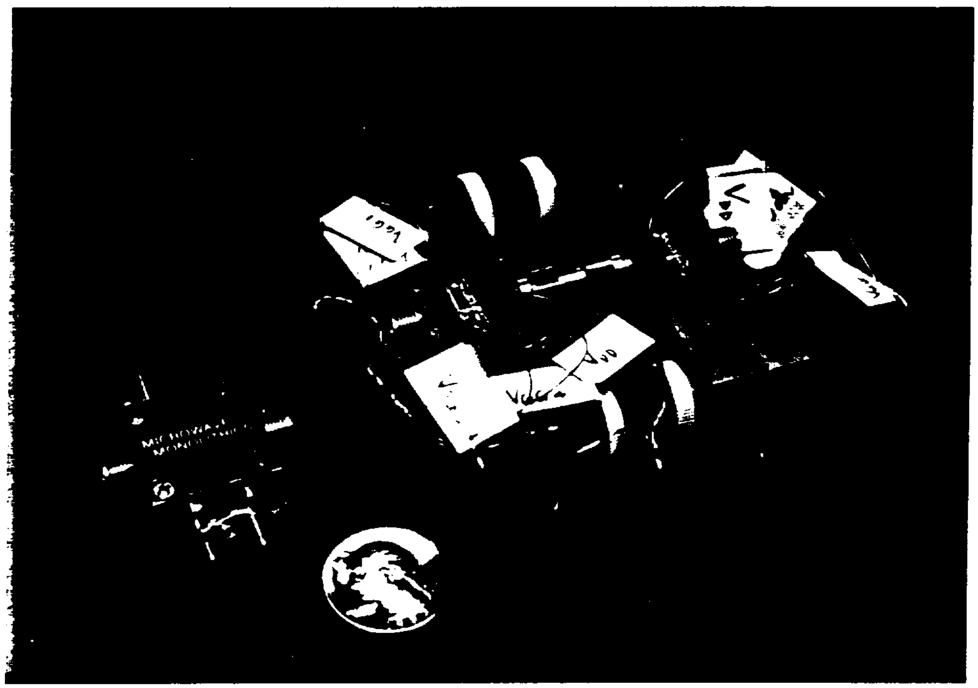

Figure 10-11 Photograph of the Components Delivered to NASA, Including the 8.3 GHz VCO with Integral Power Splitter and Divider, and the 32 GHz Divider Chain.

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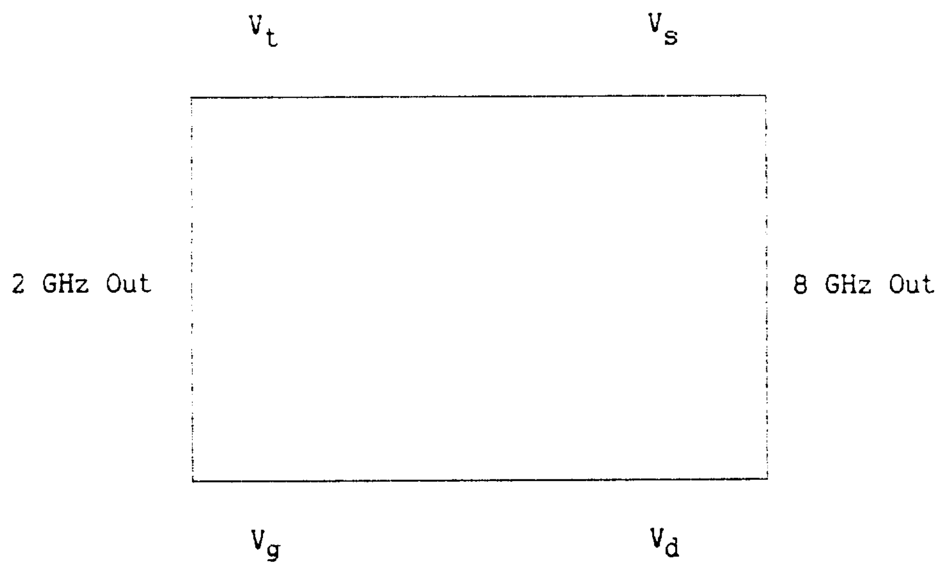

Figure 10.1-1) Pin Out Configuration for the 8.5 GHz VCO with Integral Divider.

Table 10.1-1) Measured Performance of the Integrated VCO / Dynamic Divider Delivered to NASA

V_t	F_{out}("2")	F_{out}("8")	P_{out}
-3.37 Volts	2.050 GHz	8.200 GHz	-1.6 dBm
-3.73 Volts	2.075 GHz	8.300 GHz	-2.3 dBm
-4.55 Volts	2.100 GHz	8.400 GHz	-4.0 dBm
-4.74 Volts	2.104 GHz	8.415 GHz	-4.5 GHz
-5.51 Volts	2.110 GHz	8.440 GHz	-7.5 dBm

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Table 10.1-2) Maximum Operating Limits and Operating Procedure for the Integrated VCO / Dynamic Divider.

Turn-On Sequence:

1) Set V_g to desired value:
   -2.0 Volts Min., -1.1 Volts Nominal, -0.0 Volts Max.
2) Set V_d to the desired value:
   0.0 Volts Min., 4.5 Volts Nominal, 5.0 Volts Max.
3) Set V_t offset to desired value:
   -5.7 Volts Min., -3.0 Volts Max.
4) Set V_s to desired value:
   -5.5 Volts Min., -5.0 Volts Nominal, -0.0 Volts Max.
5) Enable Phase Locking, Tuning Control must not exceed:
   -5.7 Volts Min., -3.0 Volts Max.

Turn-Off Sequence:

1) Disable Phase Locking
2) Set V_s to Zero Volts.
3) Set V_t offset to Zero Volts.
4) Set V_d to Zero Volts.
5) Set V_g to Zero Volts.

Other Precautions:

1) The chips are mounted on a copper test carrier with a thermal expansion coefficient much different than GaAs, therefore they should NOT be temperature cycled.

2) The V_g and V_t control lines are connected to the gates of small GaAs FETs and are susceptible to static discharge damage. As delivered, the test leads have shorting wires for protection which must be removed prior to operation.

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10.2) 32 GHz / 8 GHz Divider Chain

The first iteration 32 GHz divider, which actually operates at 24.5 GHz, and an additional 8.5 GHz dynamic divider were mounted on test carriers, inserted in individual test fixtures, cascaded to form a single unit, and delivered to NASA for engineering data correlation. The turn-on sequence for these circuits is described in Table 10.2-1.

Table 10.2-1) Maximum Operating Limits and Operating Procedure for the 32 / 8 GHz Dynamic Divider Chain.

Turn-On Sequence:

1) Set all V_g to desired value:
   -2.0 Volts Min., -0.0 Volts Max.
2) Set all V_d to the desired value:
   0.0 Volts Min., 5.0 Volts Max.

Turn-Off Sequence:

1) Set all V_d to Zero Volts.
2) Set all V_g to Zero Volts.

Other Precautions:

1) The chips are mounted on a copper test carrier with a thermal expansion coefficient much different than GaAs, therefore they should NOT be temperature cycled.

2) All V_g control lines are connected to the gates of small GaAs FETs and are susceptible to static discharge damage. As delivered, the test leads have shorting wires for protection which must be removed prior to operation.

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Measured performance of the 32 GHz divider is summarized in Table 10.2-2 for the following bias conditions:

V_{g1} = -0.95 Volts
V_{g2} = -0.65 Volts
V_{g1} = -0.65 Volts
V_{g1} = -0.95 Volts
V_d = 4.20 Volts @ 70 milliamps.

All gate bias lines draw just microamps of current. Bias lines are labeled on the test carrier.

Table 10.2-2) Measured Performance for the 32 GHz Dynamic Divider Delivered to NASA as Part of the Divider Chain.

Input Power Level	+12 dBm
Minimum Input Frequency for Lock*	24.08 GHz
Maximum Input Frequency for Lock*	24.80 GHz

* Input Power Dependent

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Measured performance of the 8.5 GHz divider is summarized in Table 10.2-3 for the following bias conditions:

All V_g = -1.10 Volts
V_d = 5.00 Volts @ 78 milliamps

All gate bias lines draw just microamps of current. Bias lines are labeled on the test carrier.

Table 10.2-3) Measured Performance for the 8 GHz Dynamic Divider Delivered to NASA as Part of the Divider Chain.

Input Power Level	+3.5 dBm
Minimum Input Frequency for Lock*	7.72 GHz
Maximum Input Frequency for Lock*	8.50 GHz

* Input Power Dependent

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